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RESEARCH ARTICLE

DESIGN AND IMPLIMENTAION OF VOLTAGE CONTROL OSCILLATOR WITH DOUBLE TAIL DYNAMIC COMPARATOR

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ABSTRACT

The need for low-power, area efficient, high speed VCO is pushing toward the use of dynamic regenerative oscillators to maximize speed and power efficiency. In this paper, an analysis on the fast frequency of the dynamic VCO will be presented and analytical expressions are derived. From the analytical expressions, designers can obtain an intuition about the main contributors to the vco, delay and fully explore the tradeoffs in dynamic vco design. Based on the presented analysis, a new dynamic VCO is presented by using dynamic double tail comparator. The entire design flow has been done by using Tanner EDA Tool in 180 nano meter technology.

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INTRODUCTION

Voltage controlled oscillator is a circuit that provides varying output signals (typically a square wave or triangular wave form) whose frequency can be adjusted over a range controlled by dc voltage. An example of a VCO is 566 Ic Unit, which contains circuitary to generate both square wave and triangular wave signals whose frequency is set by a external resister and capacitor and then varied by applied dc voltage. 566 Ic contains current sources to charge and discharge external capacitor c1 at arate set by external capacitor R1 and control the input dc voltage. Schmitt trigger circuit used to switch the current sources from charging and discharging the capacitor and triangualr wave devolped across the capacitor and square wave is generated at schemitt trigger are provided as outputs through buffer amplifier circuit.

Comparator

COMPARATOR is one of the fundamental building blocks in most Voltage controlled Oscillators. Voltage controlled Oscillators require high-speed, low power comparators with small chip area. High-speed comparators in ultra deep sub micrometer (UDSM) CMOS technologies suffer from low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes. Hence, designing high-speed comparators is more challenging when the supply voltage is smaller. In other words, in a given technology, to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. Besides, low-voltage operation results in limited common-mode input range, which is important in many high-speed Voltage controlled Oscillators. Many techniques, such as supply boosting methods techniques employing body-driven transistors current-mode design and those using silicon dioxide processes, which can handle higher supply voltages have been developed to meet the low-voltage design challenges. Boosting and bootstrapping are two techniques based on augmenting the supply, reference, or clock voltage to address input-range and switching problems. These are effective techniques, but they introduce reliability issues especially in UDSM CMOS technologies. Body-driven technique adopted by Blalock removes the threshold voltage requirement such that body driven MOSFET operates as a depletion-type device. Based on this approach, a 1-bit quantizer for modulators is proposed. Despite the advantages, the body driven transistor suffers from smaller transconductance (equal to gmb of the transistor) compared to its gate-driven counterpart While special fabrication process, such as deep n-well is required to have both nMOS and pMOS transistors operate in the body-driven configuration. Apart from technological modifications, developing new circuit structures which avoid stacking too

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many transistors between the supply rails is preferable for low-voltage operation, especially if they do not increase the circuit complexity. Additional circuitry is added to the conventional dynamic comparator to enhance the comparator speed in low supply voltages.

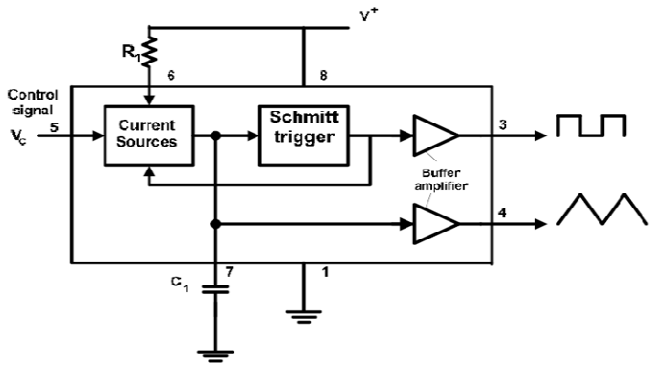
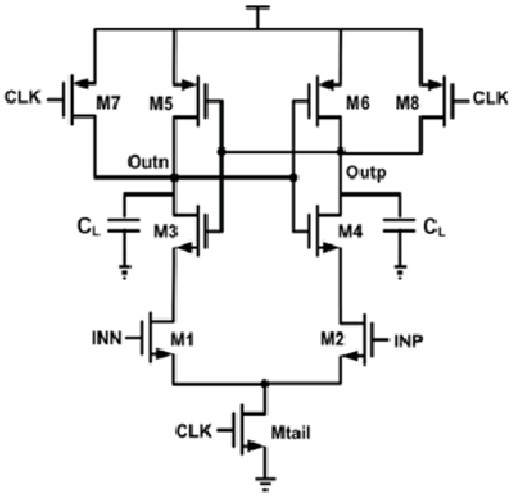


Fig.(1) A block diagram of 566 IC.

The proposed comparator works down to a supply voltage of 0.5 with a maximum clock frequency of 600 MHz and consumes18 μW. Despite the effectiveness of this approach, the effect of component mismatch in the additional circuitry on the performance of the comparator should be considered. The structure of double-tail dynamic comparator first proposed based on designing a separate input and cross coupled stage. This separation enables fast operation over a wide common-mode and supply voltage range. In this paper implemeted the design of Vco with opartional transister amplifier and double tail comparator with low voltage low power area efficient heigh performance.



Schematic diagram of the conventional dynamic comparator.

Operational Amplifier

Operational amplifier is high gain amplifier. It is a versatile device can be used amplify dc as well as input signals. It was originally designed for computing mathmatical functions such as addition, subtraction, multiplication, integration. That is the reason it is called as operational amplifier. The operational amplifier as two inputs and only one output. One input called inverting input and is denoted by minus sign. The signal applied to this input is amlified and phase inverted signal at the output is amplified signal which as same phase of the input signal.

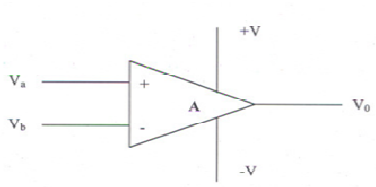


Fig. Op-amp schematic diagram

The availability of two input terminals simplifies the feedback circutary and makes the operational amplifier is very versatile device. If the feedback applied from the output to the inverting input terminal the result is negative feedback which gives a stable amplifier with precisely controlled gain characteristics, on the other hand feedback applied to inverting input, the result is positive feedback which gives oscillators and multivibrators. Special effects are obtained by combination of both types of feed backs.

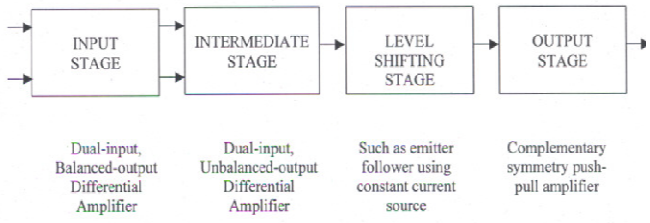
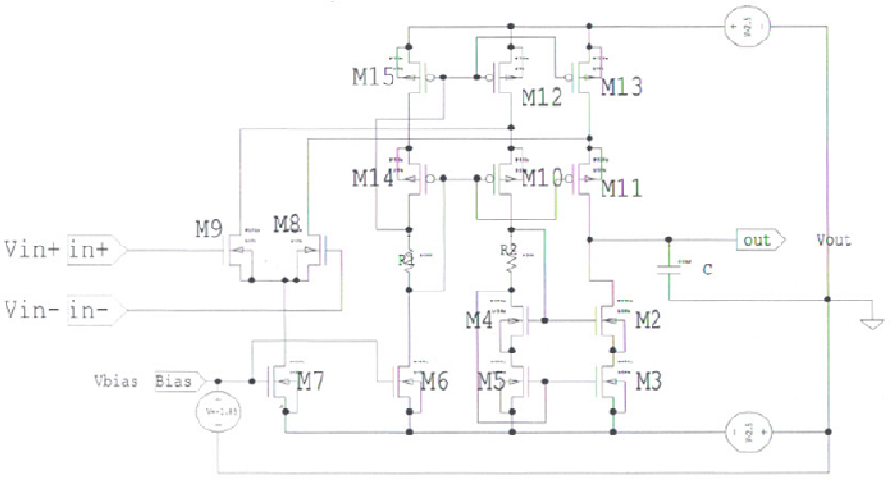


Fig. Block diagram of Op-Amp

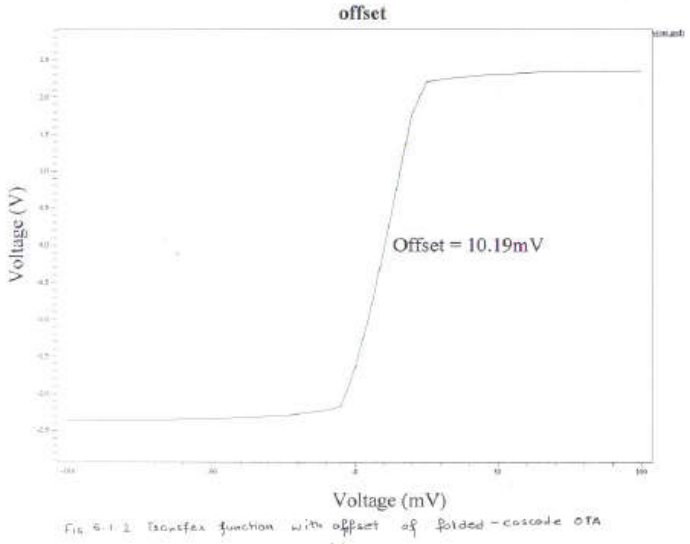
The op-amp begins with a differential amplifier stage, which operates in the differential mode. Thus the inputs noted with '+' & '- '. The positive sign is for the non-inverting input and negative is for the inverting input. The non-inverting input is the ac signal (or dc) applied to the differential amplifier which produces the same polarity of the signal at the output of op-amp. The inverting signal input is the ac signal (or dc) applied to the differential amplifier. This produces a 180 degrees out of phase signal at the output. The inverting and non-inverting inputs are provided to the input stage which is a dual input, balanced output differential amplifier. The voltage gain required for the amplifier is provided in this stage along with the input resistance for the op-amp. The output of the initial stage is given to the intermediate stage, which is driven by the output of the input stage. In this stage direct coupling is used, which makes the dc voltage at the output of the intermediate stage above ground potential. Therefore, the dc level at its output must be shifted down to 0Volts with respect to the ground. For this, the level shifting stage is used where usually an emitter follower with the constant current source is applied. The level shifted signal is then given to the output stage where a push-pull amplifier increases the output voltage swing of the signal and also increases the current supplying capability of the op-amp. The folded cascode Opamp is useful for moderately low supply voltages, at the cost of some extra current, but has limited performance in sub 1V applications, as well as a limited Vcm (in). Avdantages of folded cascode amplifier are High Gain, Improved Bandwidth, High Slew rate, High stability, High input impedance.

Dynamic comparator

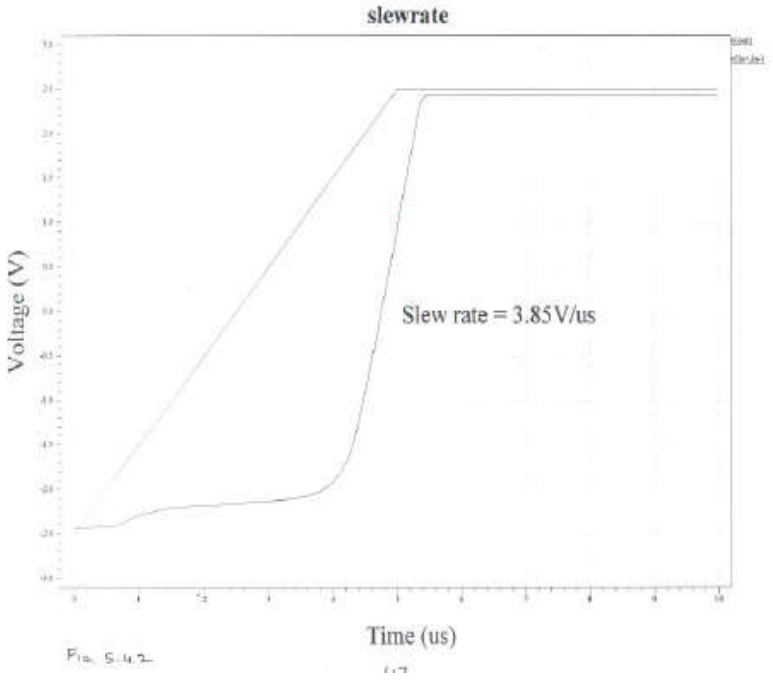
Due to the better performance of double-tail architecture in low-voltage applications, the proposed comparator is designed based on the double-tail structure.



Schematic of folded cascode of OTA



Tranfer function with offset of folded cascode Ota



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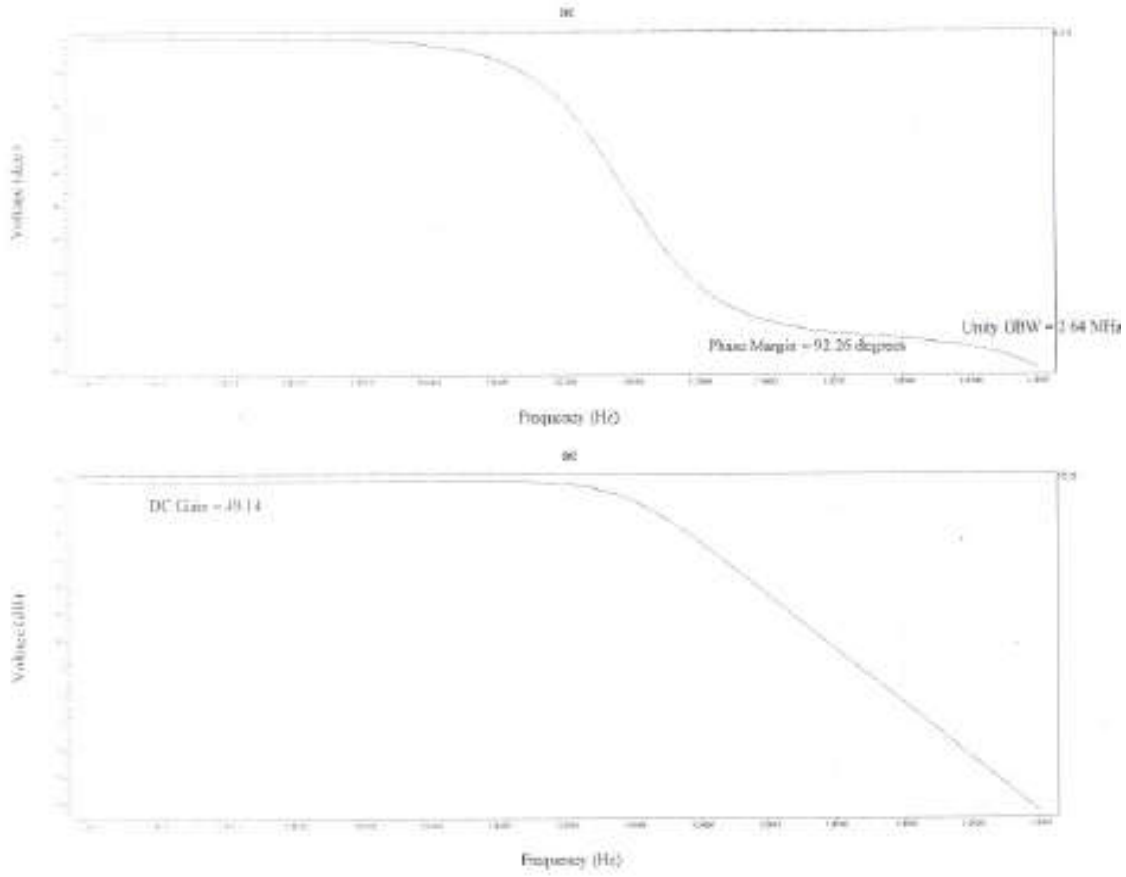


Please fig remove Ac analysis at 7Mhz design

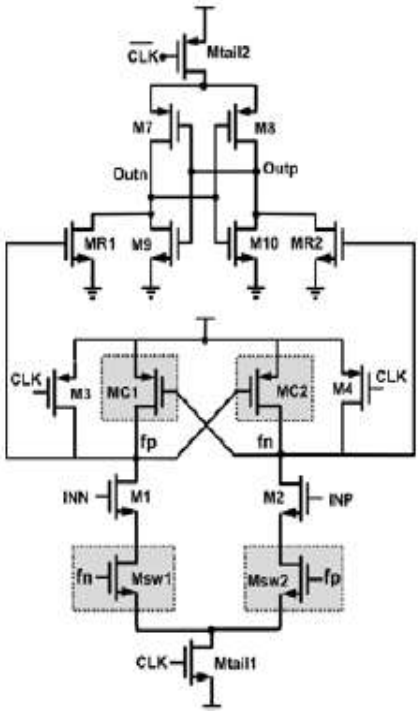
The main idea of the proposed comparator is to increase V fn/fp in order to increase the latch regeneration speed. For this purpose, two control transistors (M c1 and M c2) have been added to the first stage in parallel to M 3 /M 4 transistors but in a cross-coupled manner

A. Operation of the Proposed Comparator

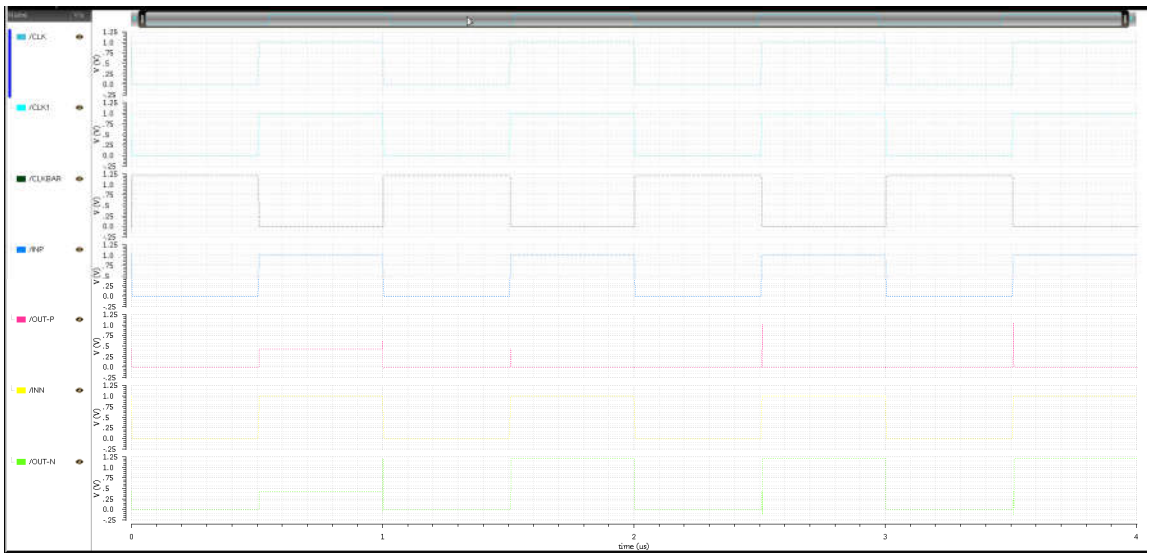
The operation of the proposed comparator is as follows. During reset phase (CLK = 0, M tail1 and M tail2 are off, avoiding static power), M 3 and M 4 pulls both fn and fp nodes to V DD, hence transistor M c1 and M c2 are cut off. Intermediate stage transistors, M R1 and M R2, reset both latch outputs to ground. During decision-making phase (CLK = V DD, M tail1 and M tail2 are on), transistors M 3 and M 4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about V DD). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose V INP > V INN, thus fn drops faster than fp, (since M 2 provides more current than M 1). As long as fn continues falling, the corresponding pMOS control transistor (M c1 in this case) starts to turn on, pulling fp node back to the V DD; so another control transistor (M c2) remains off, allowing fn to be discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which V fn/fp is just a function of input transistor transconductance and input voltage difference, in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a pMOS transistor (M c1) turns on, pulling the other node fp back to the V DD. Therefore by the time passing, the difference between fn and fp (V fn/fp) increases in an exponential manner, leading to the reduction of latch regeneration time (this will be shown in Section III-B). Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit, when one of the control transistors (e.g., M c1) turns on, a current from V DD is drawn to the ground via input and tail transistor (e.g., M c1, M1, and M tail1), resulting in static power consumption. To overcome this issue, two nMOS switches are used below the input transistors. At the beginning of the decision making phase, due to the fact that both fn and fp nodes have been pre-charged to V DD Fig. 6. Transient simulations of the proposed double-tail dynamic comparator for input voltage difference of V in = 5 mV, V cm = 0.7 V, and V DD = 0.8 V. (during the reset phase), both switches are closed and fn and fp start to drop with different discharging rates. As soon as the comparator detects that one of the fn/fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Suppose that fp is pulling up to the V DD and fn should be discharged completely, hence the switch in the charging path of fp will be opened (in order to prevent any current drawn from V DD) but the other switch connected to fn will be closed to allow the complete discharge of fn node. In other words, the operation of the control transistors with the switches emulates the operation of the latch. This will be more discussed in the following section.

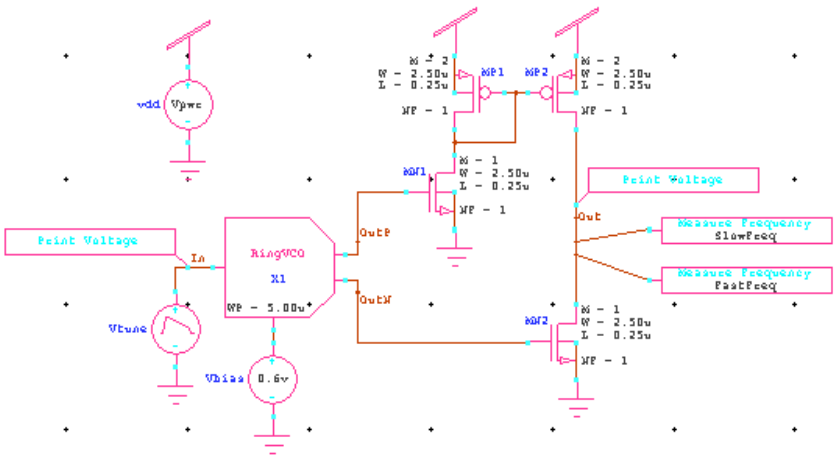
Double Tail comparator Specifications

Supply Voltage:- 1.2 v(Vdd)
Frequency of Clock:- 1.1 GHz
Technology :- 180 nm
Transient Time period :- 4ns
Power:- 18.4E-6 watt



System design with system design and VCO layout simultaneously





Full layout Design of VCO

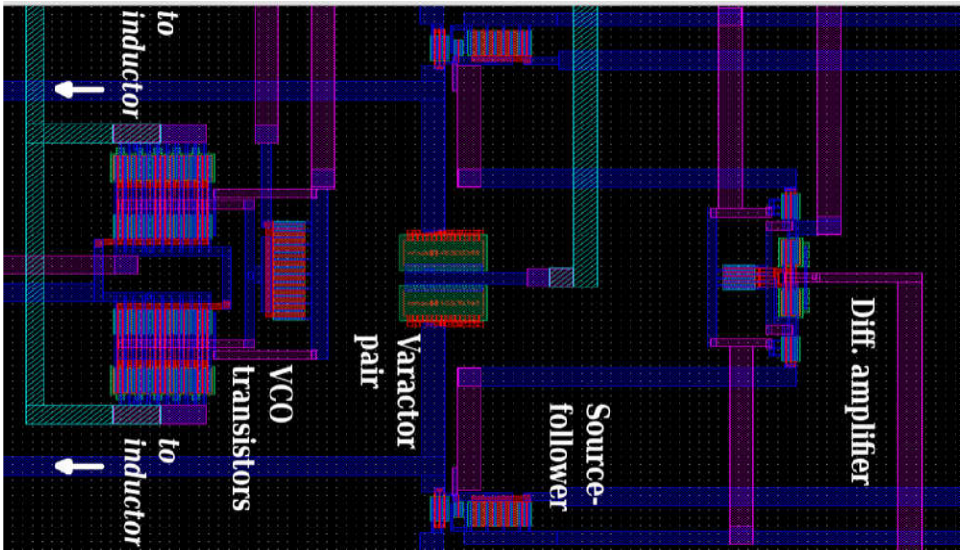
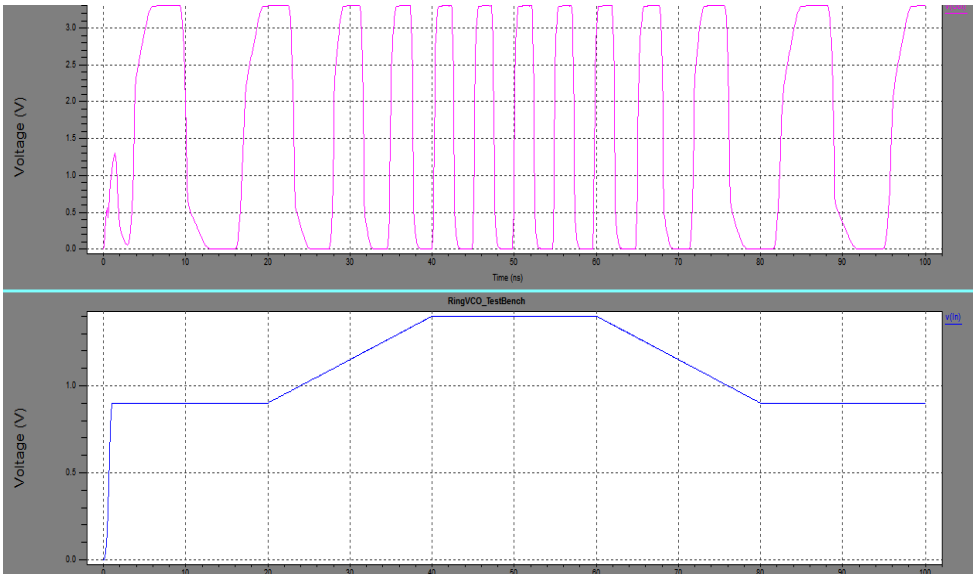


Fig: VCO Layout



System Design

system design can be observed in given diagram wich contains Source follower (external bias). Differential Amplifier (external bias). Inverter chain

Simulation Results

Simulations show a center frequency of around 1 GHz, instead of 433 MHz as designed in the referenced dissertation No varactor parasitics considered; bias voltage unknown Around 4.3% tunability with certain assumptions about inductor parasitics Varactor trade-off: Too small reduces tunability range; too large prevents oscillation

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