Available online at http://www.journalcra.com

International Journal of Current Research
Vol. 8, Issue, 09, pp.38747-38749, September, 2016

INTERNATIONAL JOURNAL OF CURRENT RESEARCH

ISSN: 0975-833X

RESEARCH ARTICLE

HDL DESIGN FOR TERA HERTZ CLOCK BASED 2E7-1 TERA BITS PER SECOND (TBPS)- PRBS SOFT A.S.I.C I.P CORE GENERATOR FOR ULTRA HIGH SPEED WIRELESS PRODUCTS

***,[1]Sastry, P. N. V. M., [2]Dr. Vathsal, S. and [3]Dr. Rao, D. N.**

[1]Professor & Dean – IT EDA Software MNC Industry & R&D CELL & ECE Dept, J.B.R.E.C
[2]Former Dean – R&D – J.B.I.E.T & Professor -AERO Dept., I.A.R.E
[3]Former Principal –J.B.R.E.C & Professor& Head –E.C.E -J.B.I.E.T

ARTICLE INFO

Article History:
Received 22nd June, 2016
Received in revised form
24th July, 2016
Accepted 07th August, 2016
Published online 30th September, 2016

Key words:

CCITT – Consulting Committee for International Telegraph & Telecom,
ITU – International Telecom Unit,
RTL- Register Transfer Level,
LFSR-Linear Feedback Shift Register,
VHDL- Very High Speed Integrated Circuit Hardware Description Language,
PRBS-Pseudo Random Binary Sequence.

ABSTRACT

The Design is mainly Intended for High Speed Random Frequency Carrier Wave Generator of 1 Tbps Data Rate using $2e^7$-1 Tapped PRBS Pattern Sequence. The PRBS is Designed by using LFSR Linear Feed Back Shift Register & XOR Gate with Specific Tapping Points as per CCITT ITU Standards. RTL Design Architecture Implemented by using VHDL &/ Verilog HDL, Programming & Debugging Done by using Spartan III FPGA Kit. Transmission done through this carrier frequency. Propagation Carrier Done either Serially / Parallel lines I/O.

Citation: Sastry, P.N.V.M., Dr. Vathsal, S. and Dr. Rao, D.N., 2016. "Hdl design for tera hertz clock based $2e^7$-1 tera bits per second (tbps)- prbs ip core generator for ultra high speed wireless products", *International Journal of Current Research*, 8, (09), 38747-38749.

INTRODUCTION

In Modern Hi-tech Communication Engineering world, High Speed based Portable Communication System Hardware & Software Products Came to the market, speed is an important factor and is in terms of Giga bits per second for all Hi-tech Real time Smart Computing Portable wireless Communication System Software products like Cloud Computing ,wireless Internet Data Packets Transceivers Computing, Tablets, Pocket Mobile Multimedia Systems, Note Book Computers, Wireless Routers, N.O.Cs, Network Cards/ Racks, Wi-FI, Gi-Fi, Wimax, G.P.S, G.S.M, Q.C.D.M.A Tranceivers. For that purpose, I Designed Giga Bits Per Second, Tera Bits Per Second High Speed PRBS is Pseudo Random Binary Sequence Frequency Generators, Generate & Received Random Frequency Data in the form of Random frequency numbers of different speed w.r.t specific Data tapping sequence points for both signal & carrier wave generation. P.R.B.S Generators, Receivers, Transceivers Designed for Hi-Fi Wireless Internet Data Packets Computing and Cloud Computing etc. Transmission, Reception of Data is in the RANDOM Sense, This PRBS Generator, Receiver is Designed for Identification property of Different Tapped PRBS Sequences like 7, 10, 15, 23, 31 at a Clock carrier frequency speed of Tbps/Pbps. The Length of PRBS sequence is 2^L-1. 2^L-1 times repeated the sequences. this is mainly suit for multiple users to transmit and received data in accurate time for very long distance communications like GPS Data Acquisition, GSM Communication Systems, Wi-FI,Gi-FI, LTE, Wireless O.F.D.M.A, C.D.M.A,Q.C.D.M.A Computing, wireless internet computing, cloud computing etc because of Ultra High speed Communication Rate in terms Gbps, Tbps, P.b.p.s. All these P.R.B.S L.F.S.R Sequences are designed by tapping different points according to I.T.U O.150,O.151, O.152 Standards. This P.R.B.S Design Consists of Multiplexer, P.R.B.S Registers of different tapped sequence points, Clock Frequency Generators of Tbps/Pbps Speed. The

****Corresponding author: Sastry, P.N.V.M.,***
Professor & Dean – IT EDA Software MNC Industry & R&D CELL & ECE Dept, J.B.R.E.C

Advantages of these P.R.B.S Generators having In Built Checkers, Bit Error Rate Detection & Correction by using P.R.B.S Checkers. These are simply Linear Polynomial Checkers & C.R.C.

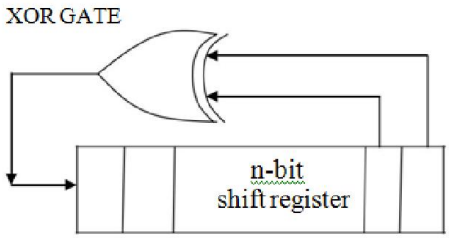


Figure 1. P.R.B.S DESIGN -Fibonacci (many-to-one) realization of L.F.S.R with minimum number of taps and XOR gate in its feedback

Software – V.L.S.I I.C Design flow

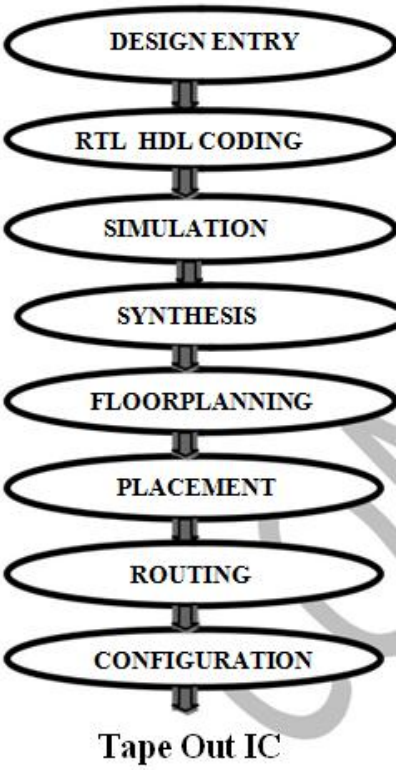


Figure 3. VLSI IC Design Flow Chart

$2e^7$-1 Tera Bits Per Second (Tbps) PRBS Design

Tera Bits per Second Clock

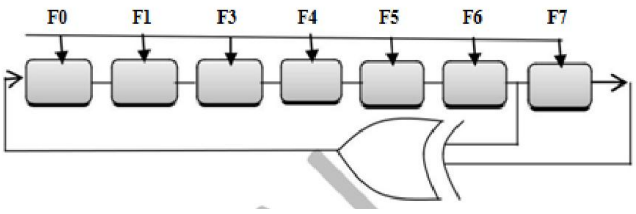
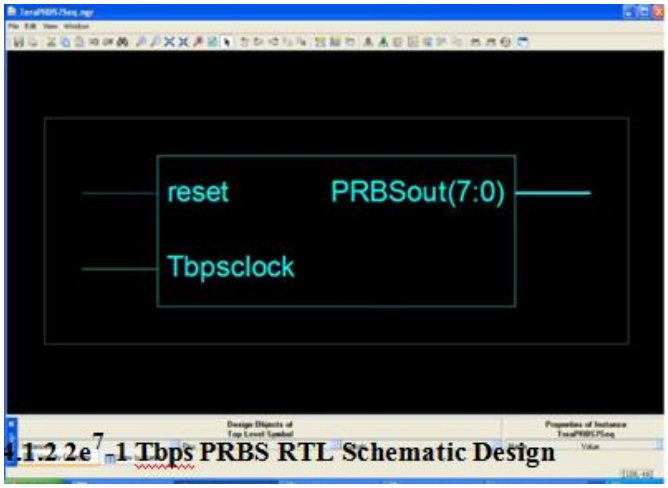


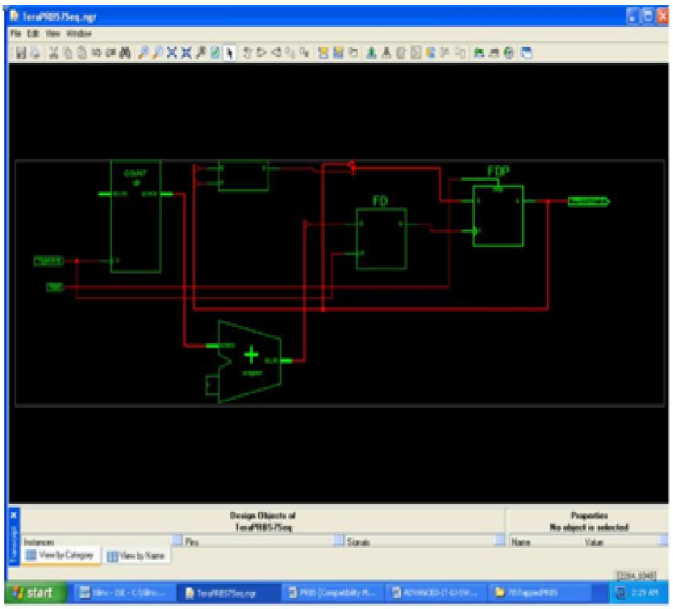
Figure 2. $2e^7$-1 PRBS Design

Design Flow Reports

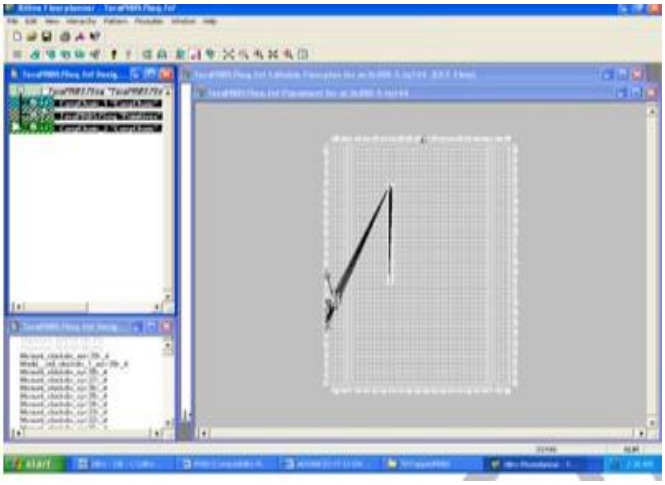
$2e^7$-1 Tbps P.R.B.S design R.T.L block



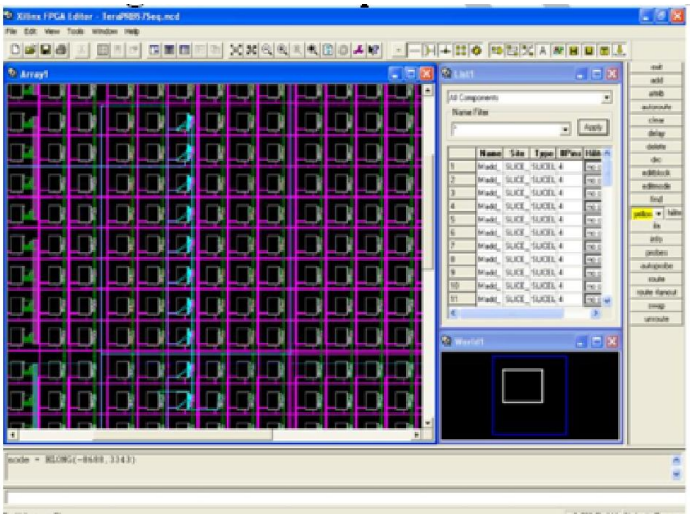
4.1.2 $2e^7$-1 Tbps PRBS RTL Schematic Design



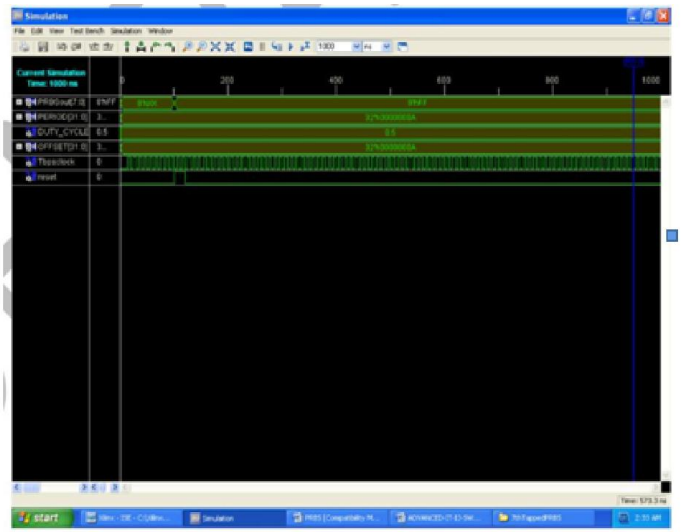
Design Placed Report



Design Routed Report



Simulation wave form results



Conclusion

Designed 2e7-1 Tbps PRBS for Ultra High Speed Wireless Communications.

****

REFERENCES

"ITU-T Recommendations O151, O152 and O153," Tech. Rep.

Ahmad A. and Elabdalla A. M., "An efficient method to determine linear feedback connections in shift registers that generate maximal length pseudo-random up and down binary sequences," *Computer & Electrical Engineering - An Int'l Journal (USA),* vol. 23, no. 1, pp. 33-39, 1997 [7] Ahmad, A., Al Musharafi, M.J.,

Ahmad, A., Nanda, N. K., and Garg, K., "An efficient design of maximal length of pseudorandom test pattern generators," *Proceedings of IEEE international conference on signals & systems.*

Alfke, P. "Efficient Shift Registers, LFSR , Counters and Long Pseudo-Random Sequence Generators," XAPP 052, July 7, 1996 (Version 1.1)

Annie Xiang, Datao Gong, Suen Hou,Chonghan Liu, Futian Liang, Tiankuan Liu, Da-Shung Su, Ping-kun Teng, Jingbo Ye, "Design and verification of an FPGA based bit error rate tester", Elsevier, Physics Procedia, 2011.

HDL Chip Design, Douglas J. Smith, Doone Publications, 1996

http://en.wikipedia.org/wiki/ Linear_feedback_shift_register

https://www.verigy.com/help/topic/com.verigy.itee.help. smartest.ui.7.1.0/95305.htm

Hwang SY, GY Park, DH Kim, KS Jhang, "Efficient Implementation of a Pseudorandom Sequence Generator for High-Speed Data Communications", ETRI Journal, Volume 32, Number 2, April 2010.

Panda Amit K, Rajput P, Shukla B, "FPGA Implementation of 8, 16 and 32 Bit LFSR with Maximum Length Feedback Polynomial using VHDL", 2012 International Conference on Communication Systems and Network Technologies.

Proakis J. G. and M. Salehi, "Digital Communications, Fifth Edition," Mc Graw-Hill International Edition, New York, US, 2008.

Wikipedia, http://en.wikipedia.org/wiki/Pseudorandom_binary _sequence

Xilinx Data Sheet XAPP884 (v1.0) January 10, 2011