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RESEARCH ARTICLE

IMPLEMENTAION OF SERDES FOR OPTICAL DATA ACQUISITION-CATH LAB

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ABSTRACT

A catheterization laboratory or Cathlab is an examination room in a hospital that offers a variety of diagnostic and interventional cardiology procedures used in the treatment of coronary artery and peripheral vascular diseases. The diagnostic imaging equipment of the Cathlab is used to visualize the arteries and chambers of the heart and treat any stenosis found. In the Cathlab data is send through optical fiber cable to the acquisition computer. The acquisition computer consists of digital processing board. Optical cable from x-ray detector is connected to the detector interface and processing board (DIPB). This board uses an optical transceiver to convert optical data into digital data. As the transceiver data is serial this is converted into parallel data using SerDes chip. This is fed to FPGA for imaging processing. The SerDes chip VSC7145 used to convert serial data into parallel data is obsolete and no more available for manufacturing. There is no direct replacement of this part. This paper explains an alternate all digital design for SerDes chip that to be used in the cathlab system.

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INTRODUCTION

The SerDes chip VSC7145 is a dual speed fiber channel, Gigabit Ethernet, and infiniband serializer/deserialzer (SerDes) optimized for power and performance in an industry standard pin out. The SerDes chip accepts 10 bits of stub series terminated logic, 8B/10B encoded data, latches it synchronously to the transmit byte clock and serializes at baud rate which is 10,20 or 40 times the reference clock. The VSC7145 also samples the data at the receive end and recovers two clocks which is $1/10^{th}$ or $1/20^{th}$ of the baud rate. The SerDes chip is an important component in the Cath lab system. It receives digital data in serial form and convert the data into parallel form for imaging processing at the next section of the system. Earlier the chip was designed using VLSI technology and is mounted outside the system as a separate unit. The main drawback with the VLSI design is the high cost that has to be bear by the customer. This paper introduces a new design concepts for SerDes using an all digital design. One of the main advantage with the new design is that the cost can be reduced considerably and the chip can be mounted inside the system on FPGA, so that the system becomes more compact.

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Related works

The demand for high speed data transmission is increasing day by day. The high speed transmission would help in improving the I/O characteristics of a computer data links. The work done by the (Muneo Fukaishi and Kzayuki Nakamura, 1998) explains a design for a fiber channel transceiver using asynchronous tree type de-multiplexers and frequency conversion architecture. The complete design consists of a de-multiplexer,8 bits to 10 bits parallel frequency conversion circuit and a comma detection & word alignment logic. The design uses very low power compared to other previously designed systems.

The (Wen-Hu-Z *et al*., 2003) explains a CMOS word alignment circuit which works at a speed of 3.125Gb/s. The word alignment circuit is designed using de-multiplexer circuit and the design can be used for the serial data communication. The design operates at half the clock frequency of the input data and it can operate from 1Gb/s to 3.125Gb/s with 3.3V supply. The architecture is compact and it will integrate only less number of transistors. So this design will reduce the die area and power consumption greatly.

A SerDes technology for the Gigabit Ethernet communication in storage area network is given by (Iniewski *et al*., 2004). One

of the main challenge with the SerDes chip is the jitter specification. The work done by the (Iniewski *et al*., 2004) mainly review the storage area network requirement and demands. The (Chnag-Chun Zhang and Zhi –Gong Wang, 2008) presents a de-multiplexer design using the standard 0.18um CMOS technology. A conventional current mode logic (CML) is used to design the logic behind the de-multiplexer. The designed de-multiplexer can works up to 20Gb/s data rate for the optical data links. The work done by the ()also explains a low jitter multiplexer and de-multiplexer using the BiCMOS technology. The designed multiplexer/de-multiplexer can work up to 60Gb/s data rate. The mux and de-mux are driven by a quarter clock and hence reduces clock frequency circuit design complexity.

The (Yu Zhen and Hu Qing-sheng, 2011) introduces a comma detection and word alignment circuit for the high speed SerDes chip. The proposed design can work up to 6.25Gb/s. In order to increase the speed, combined parallel and pipelined architecture is employed in this design.

Block Diagram

The Cath Lab System

Fig.1 shows the DIPB of Cath Lab system. The detector of the system converts the digital data into optical data. The optical data is processed at the DIPB section of the Cath Lab.

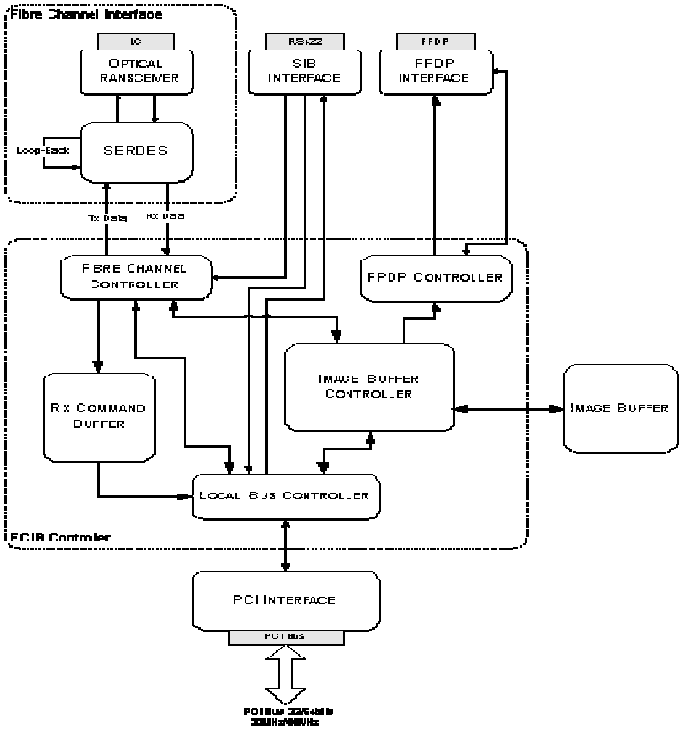

Fig.1.DIPB Block Diagram

The Front pannel data data port(FPDP) is a high speed data streaming serial communication protocol.FPDP currently supports three distinct speeds.1.0625Gb/s, 2.125Gb/s and 2.5Gb/s.It can work over long distances using optical fiber cables or shorter distances over copper cables. In cath lab systems it uses optical cable.

SerDes Chip Block Diagram

The 8bit at the input of the SerDes is encoded using 8B/10B encoding protocol. This is a line code that maps 8bit symbols to 10 bit symbols to achieve DC balance and bounded disparity. This encoding also provide enough state changes to allow reasonable clock recovery at the receiver. In this coding the difference between the counts of ones and zeros in a string of at least 20 bits is no more than two and that there are not more than five ones or zeros in row. This helps to reduce the demand for the lower bandwidth limit of the channel necessary to transfer the signal.

In 8B/10B encoding, the 8 bits of data are transmitted as a 10 bit entity called symbol or character. The low 5 bits of data are encoded into a 6 bit group portion. The top 3 bis are encoded into a 4 bit group. These coded groups are concatenated together to form the 10-bit symbol that is transmitted on the wire. It is common that the standards using the 8B/10B encoding also define up to 12 special symbols that can be send in place of a data symbol. The special characters are often used to indicate the start of frame, link idle, skip and similar link level conditions. At least one of the special character or comma character is needed to define the alignment of the 10 bit symbols. In the case of fiber channels k28.5 comma character is used at the beginning of four byte sequences that perform functions such as loop arbitration, fill words, link resets etc. At the receiving end, the receiver will check for both disparities of k28.5 character.

The clock multiplier is a PLL with a decade counter in the feedback path. The main purpose of the DFF is to synchronize the data with the internally generated clock. The input clock frequency is of 125MHz and so the internally generated clock is of 1.25GHz. The parallel to serial block convert the parallel data into serial one. The SO output formed by serializer has two modes: 1) when EWRAP is HIGH the output of the serializer is multiplexed internally to the receiver and the SO output is HIGH 2) when EWRAP is LOW, the output of the serializer is transmitted on the SO output.

When the TXRATE is high for full speed operation, the timing of this bus ASIC friendly ,meaning that TBC and T(0:9) data are generated in the protocol device in-order to facilitate compliance and hold timing. When TXRATE is LOW, the transmitter runs in the half speed and data is latched at the falling edge of the TBC. The data will be serialized and transmitted on the SO± differential output at a bit a rate that is 10,20, or 40 times the frequency of the REFCLK ,as determined by the REFRATE and the TXRATE, with T0 bit as the first bit. The SO outputs must be AC-coupled to the link. User data should be encoded using 8B/10B block code or an equivalent, run-length-limited, DC-balanced code. An encoded byte is 10 bits and is referred to as a transmission character.

The de-serializer receives data in serial form and de-serializes into 10-bit SSTL class bus along with complimentary recovered cocks that are divided version of the received clock.

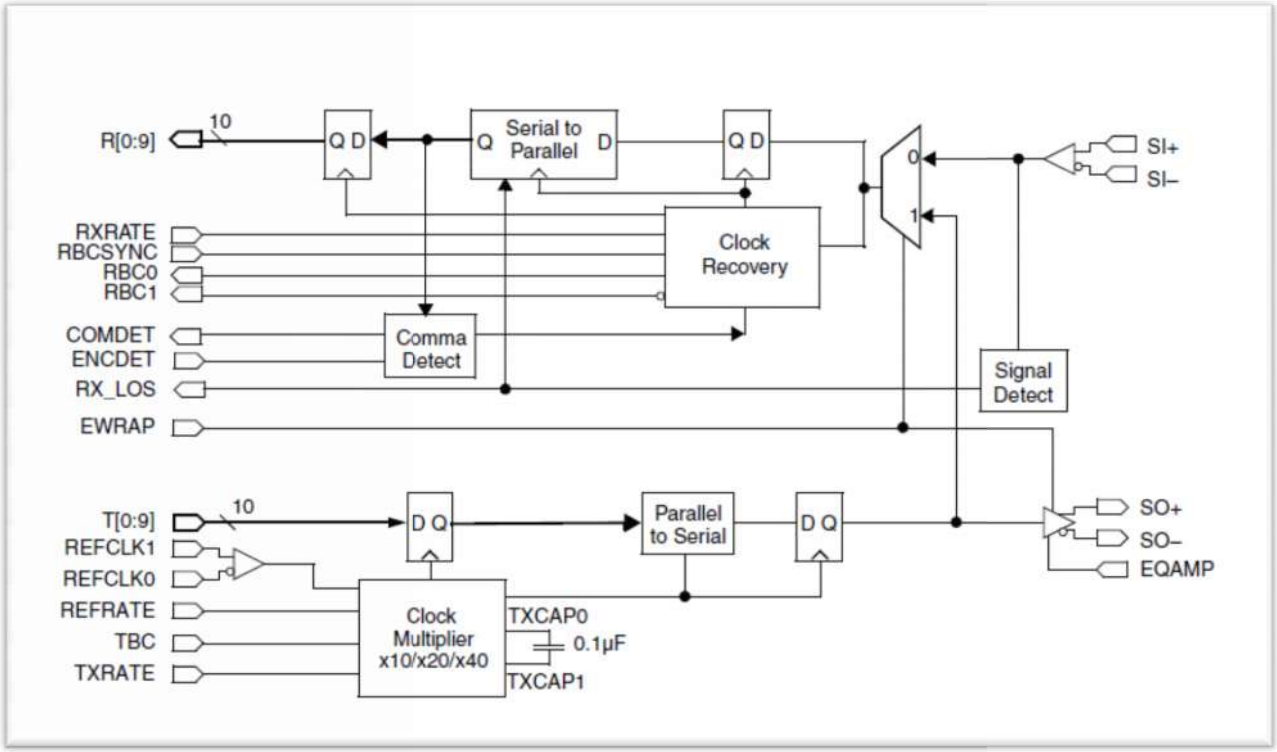

Fig.2. SerDes Block Diagram

RXRATE and RBCSYNC determine the sped of the recovered clock RBC0/RBC1. This timing relationship is shown in the Table 1.

Table 1. Receiver Operation

RXRATE	RBCSYNC	SI input rate	RBC rate	comments
0	0	1.25	65.5	Half speed mode
0	1	1.25	125	Full speed mode
1	0	2.5	125	Full speed mode
1	1	2.5	125	Full speed mode

The receiver pat of VSC7145 has an output RX_LOS which indicates (when low) that the SI input contains valid signal. Transition Detection: The circuit performs an analog detection to check the signal swings are of adequate amplitude. The SI input of SerDes has a buffer which contains a differential voltage comparator which goes low when the differential peak to peak voltage is greater than 200mV or HIGH if under 80mV. RLL Checking: In this the incoming serial data is checked for run length violation. Normally 8B/10B encoded data will not contain more than consecutive 1's or 0's. So the if the input contains more than 6 consecutive 1's or 0's, the data is invalid.

K28.5 check: In this incoming data is checked for both disparities of the k28.5 characters (0011111010 and 1100000101), regardless of the state of ENCDET. Since most of the high speed serial data streams are send without an accompanying clock the receiver generates a clock from an approximate frequency reference, and then it phase aligns to the transitions in the data stream with a PLL.

This process is called as clock and data recovery. It is an important block in the case of de-serializer.

RESULTS

The proposed design for the SerDes is simulated using Cadence Pspice model. Design models for serializer and de-serializer are simulated separately and then combined later.

The Fig.3 shows the proposed circuit diagram of serializer. The circuit is simulated for a time duration of 16ns.The flip flops are initialized to zero state and clock delay of zero is applied

The simulation results of the serializer is given in Fig. 4. Here the input data is set to 1 for 1st 10 clock duration followed by 0 for next 10 clock duration.

The one important block in the receiver is the clock and data recovery circuit. This circuit recovers the clock signal from the received data. For the clock recovery an Alexander phase detector is used. A charge pump is used at the output of the phase detector in order to convert the phase variation into a voltage variation.

The simulation result of the phase detector is given in fig.6. The simulation result shows that the voltage at the output of the charge pump is in micro voltage.

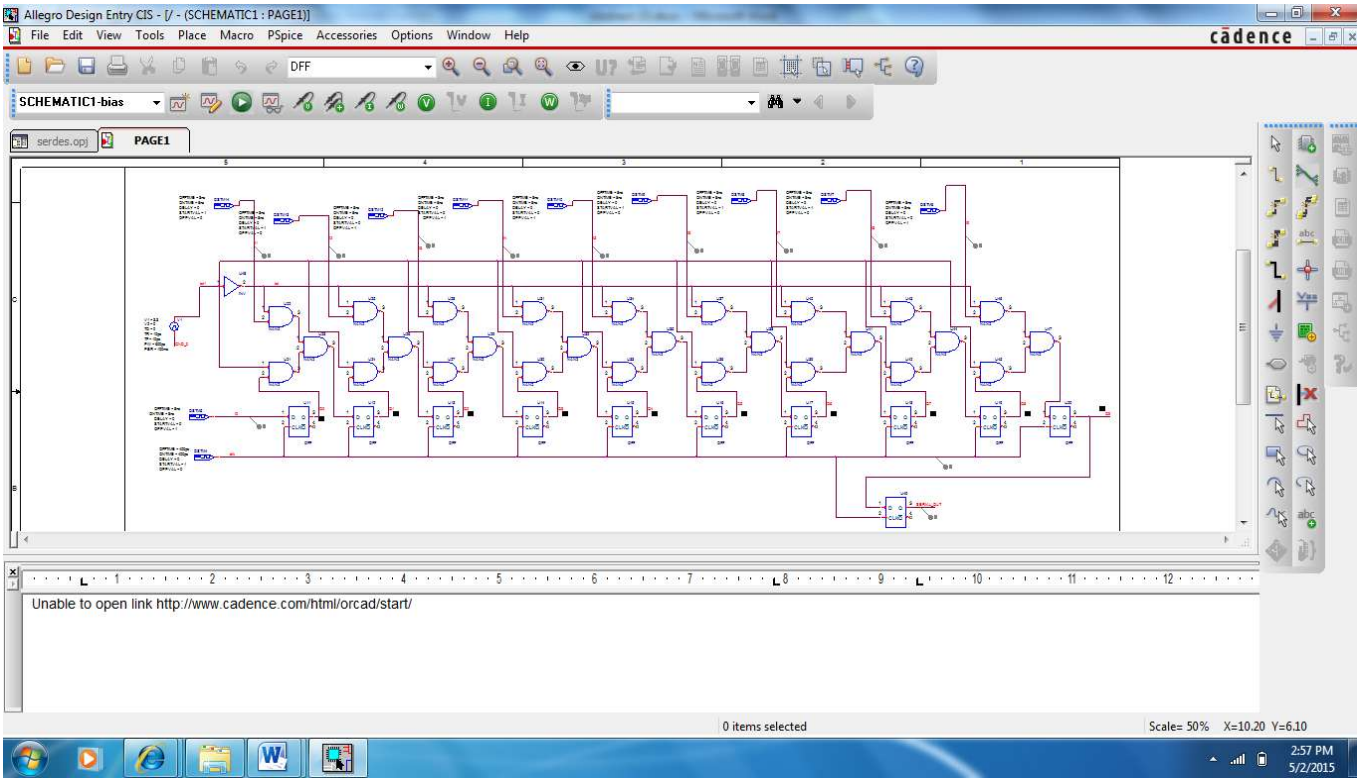

Fig.3.Circuit Diagram of Serializer

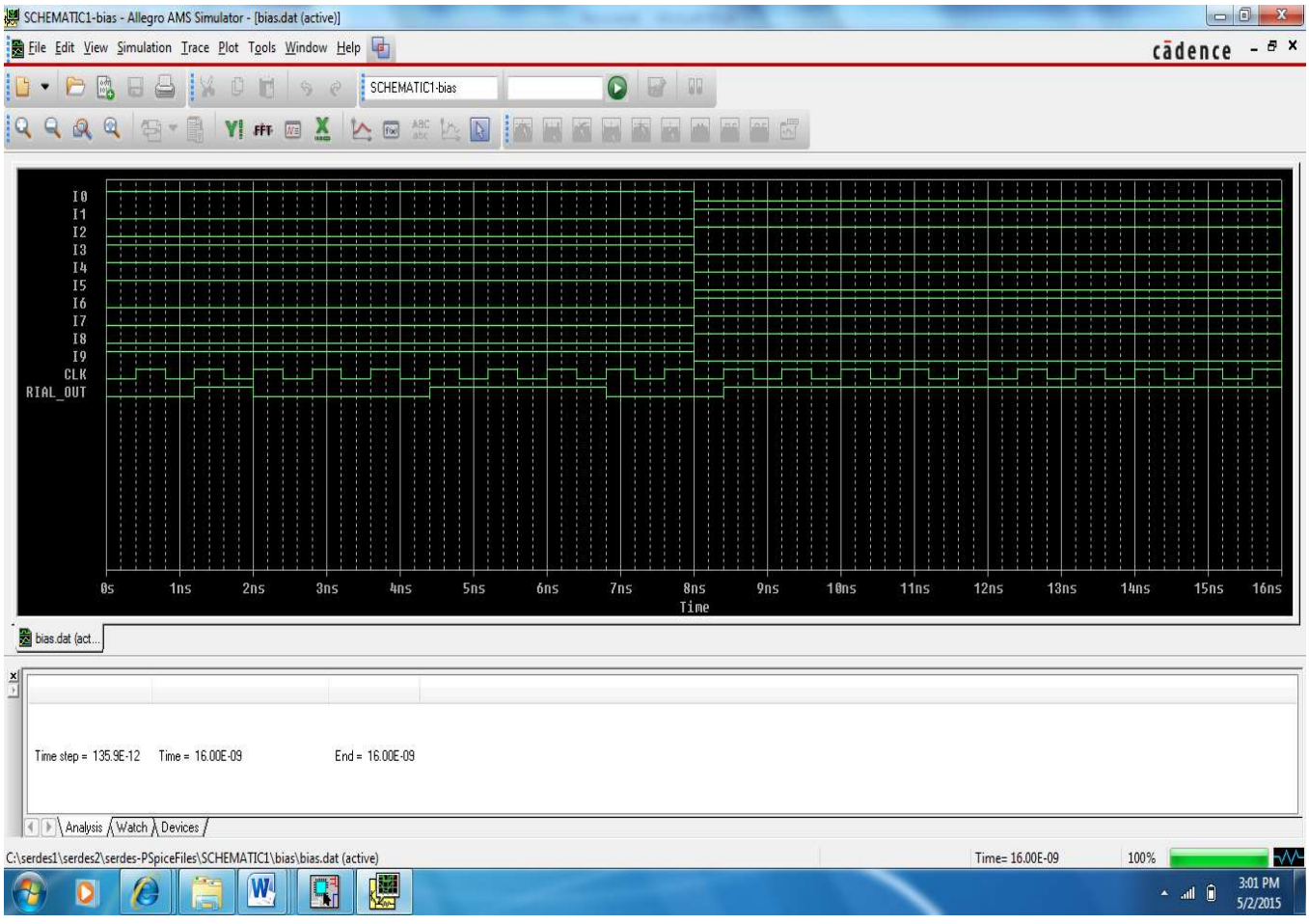

Fig.4. Simulation results of serializer

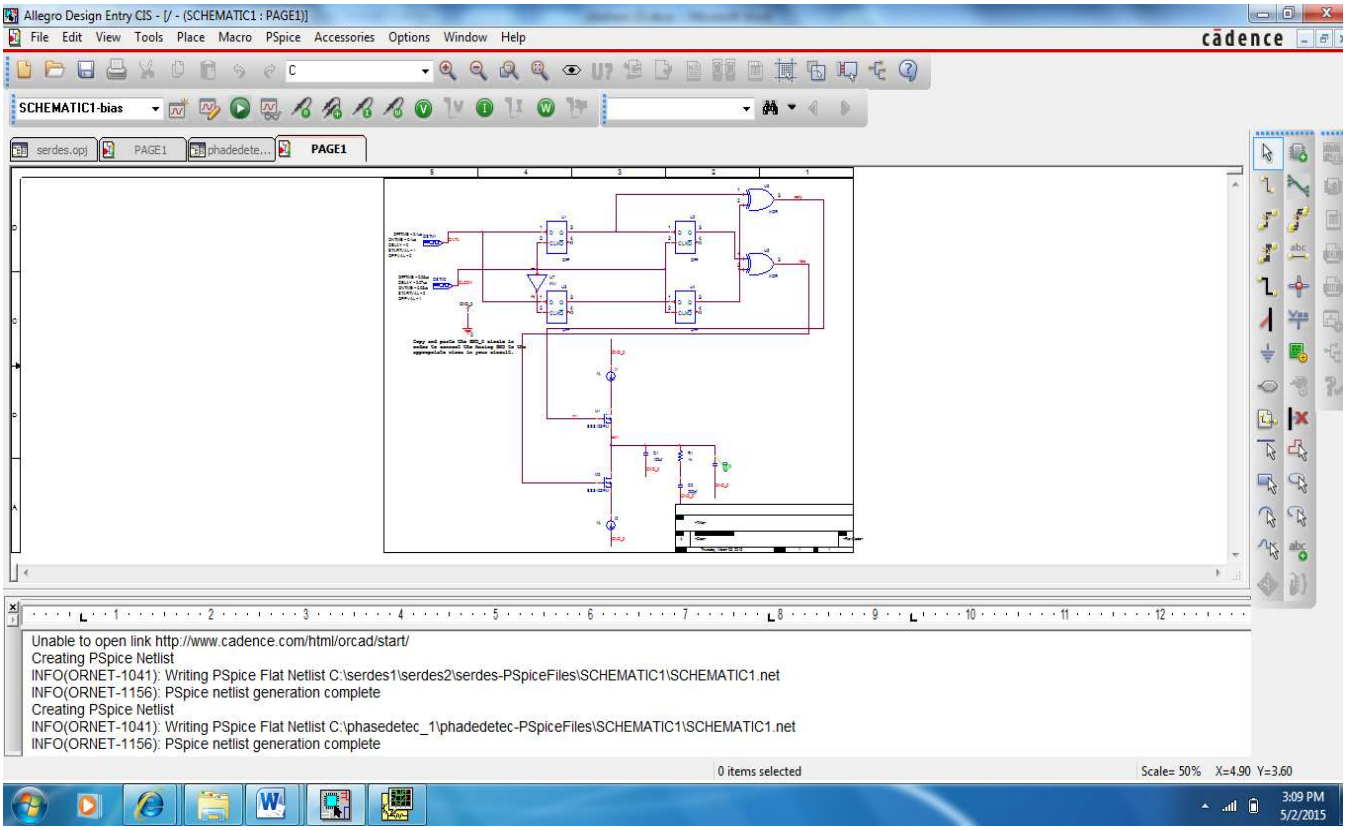

Fig.5. Phase Detector Circuit Model

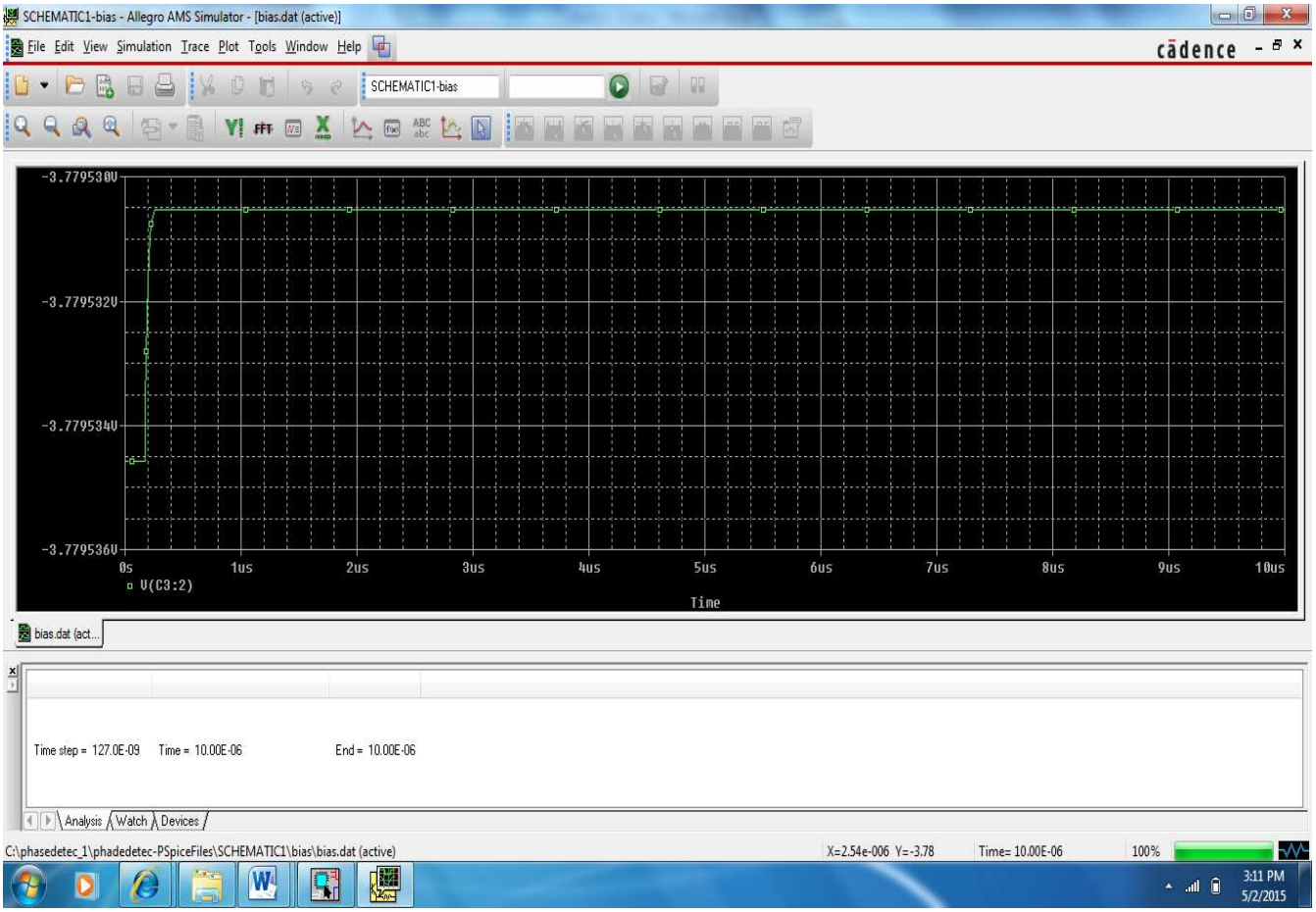

Fig.6. Phase Detector Output

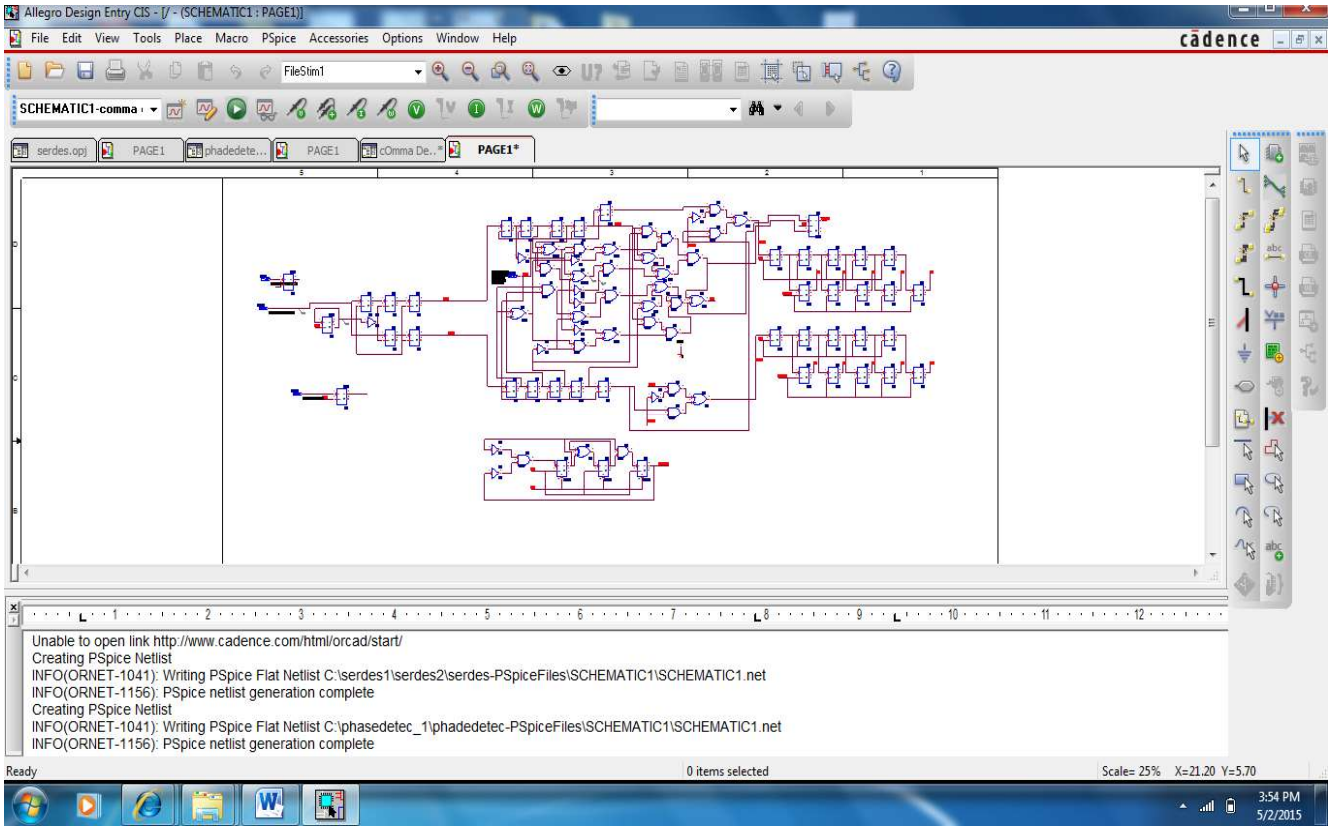

Fig.7. Proposed Comma Detection Circuit Model

Another important block in the receiver is the comma detection block. The main purpose of this block is word alignment. The word boundary is set with comma signal as reference. The proposed design model for comma detecton circuit is shown in Fig.7. The circuit takes the serial data as input and listens to the comma character. On the detection of the comma signal the clock is divided by 5 and tree type DeMux converts the data into parallel form at the output of the circuit model.

Conclusion

The proposed SerDes model gives excellent results in Pspice simulation environment.The synchronization of various components with the FPGA can be done using VHDL coding.

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