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RESEARCH ARTICLE

DESIGN OF REDUCED LOSS 5*32 DECODER USING REVERSIBLE GATES

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ABSTRACT

Reversible logic gates, in which the number of outputs is equal to number of inputs and each input, must give equal output pattern. These gates are reversible gates as it also helps in recovering inputs from outputs. The reversible 5x32 decoder consists of a reversible 4x16 decoder and fredk in gate which again consists of peres gate,one TR gate,one NOT gate, three CNOT gates,28 Fredkin gates. Reversible decoder 5x32 is designed with 4x16 decoder and fredkin gate with minimum cost, both delay and power consumption are reduced compared to normal decoder. Reversible decoder can be widely used in low power VLSI, DSP, nano computing, and optical computing.

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INTRODUCTION

According to landauer's principle Energy is dissipated due to loss information bits, the loss of one bit information will dissipate Kt*log2 joules of energy where k is the Boltzmann's constant, T is the absolute temperature, showed that reversible circuits avoids the bit information loss. The amount of energy directly related to the number of bits erased during computation. Irreversible circuits dissipate energy in the form of heat and cause to reduce the life time of circuit. Reversible circuits do not erase information and dissipate very less heat. Synthesis of reversible circuit differs from combinational circuit in many ways. Firstly, in reversible circuit there should be no fan-out, i.e. each output used only once. Secondly, for each input pattern there should be unique output pattern finally, resulting circuit must be acyclic. Reversible decoder can be widely used in low power VLSI, DSP, Nano computing, and optical computing, etc. Any reversible circuit design includes only the gates that the number of gates, quantum cost, and the number of garbage outputs.

LITERATURE SURVEY

According to Gordon .E. Moore in 1965, the number of components on the chip will double every 18 months, initially he predicted for 10 years but due to growth in technology his prediction valid today. Also predicted that the amount of power dissipated is equal to the heat dissipated by the rocket nozzle, hence power minimization has become important factor for VLSI Design environment. Landauer's principle Energy is dissipated due to loss information bits, the loss of one bit information will dissipate Kt*log2 joules of energy where k is the Boltzmann's constant, T is the absolute temperature. C .H Bennett in 1973 revealed that power dissipation can be made to zero by reversible circuits. He proved that his theory with the help of Turing machine which is symbolic model for computation introduced by Turing. In 1994 Shor did a remarkable research work in creating algorithms for reversible circuits efficiently for computing compared to classical computing. Edward Fredkin and Tommaso Toffoli introduced new reversible gates known as Fredkin and Toffoli reversible gates based on the concept of reversibility. These gates have tree inputs and three outputs and so called 3x3 reversible gates .These gates have zero power dissipation. Peres introduced new reversible gate and it is also 3x3 x reversible gates like Fredkin and Toffoli gates but it is not universal gate. It is widely used as its quantum cost is very less i.e. 4 compared other gates. H.Thalpliyal and Ranganathan introduced gates to sequential circuits such as D-latch, SR-latch,JK-latch…, using Fredkin and Feynman gates has been done. S.Chiwande prashanth R.Yelekar system gate is a 4x4 reversible gate and is used in sequential circuits.

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M.L. Chuang C.Y. Wang proposed that number of gate and number of garbage outputs can be reduced by implementing sequential circuits. Rajmohan and Dr.V. Ranganathan implemented counters using reversible logic.

In 1980, Edward Fredkin and Tommoso Toffoli developed the universal reversible gate named as Fredkin and Toffoli gate and works on reversibility with 3 inputs and 3 outputs, these gates provide no information loss and no dissipation power. Peres introduced new reversible gate and it is also 3x3 reversible gate like Fredkin and Toffoli gates but it is not universal gate. It is widely used as its quantum cost is very less i.e. 4 compared other gates.H.Thalpliyal and Ranganathan introduced gates to sequential circuits such as D-latch, SR-latch JK-latch…, using Fredkin and Feynman gates has been done. S.Chiwande prashanth r.yelekar system gate is a 4x4 reversible gate and is used in sequntial circuits.M.L.chuang C.Y.Wang proposed that number of gate and number of garbage outputs can be reduced by implementing sequential circuits. Rajmohan and Dr.V.Ranganathan implemented counters using reversible logic.

Reversible logic

The n-input and k-output Boolean function f(x1, x2, x3,) Referred to as (n, k) functions reversible if

- The number of outputs equal to number of inputs
- Each must give equal output pattern

Reversible logic gates

The gates in which the number of outputs equal to number of inputs and each must give equal output pattern. It also helps recovering inputs from outputs

Feyman Gate FG (Feyman, 1985)
Peres Gate PG (Peres, 1985)
Toffoli Gate TG (Toffoli, 1980)
Fredkin Gate FG (Fredkin and Toffoli, 1882)
Khan gate KG (Khan, 2002)
TSG Gate TSG (Thapliyal and srinivas, 2005, 2006)
MKG Gate MKG (Shanuetal, 2008)

Ancilla/Constant inputs: The number of inputs either 0 or 1 is added to the input side to synthesize logical function

Garbage outputs: These are added to the output to maintain the reversible logic i.e equal input and equal output, these outputs are mandatory to maintain reversibility.

Inputs+constant inputs=output+garbage outputs

Quantum cost: It is defined as the cost of the circuit in terms of cost of primitive gate .it is calculated by the number of primitive reversible gates (1x1 or 2x2) required to realize logic function. Quantum cost of circuit is the minimum number of 2x2 unitary gates required to keep output to be unchanged. Any reversible circuit design includes only the gates that the number of gates, quantum cost, and the number of garbage outputs. The reversible 5x32 decoder consists of a reversible 4x16 decoder and fredkin gate which again consists of Peres gate,one TR gate,one NOT gate,three CNOT gates,28 Fredkin gates.

Hardware Complexity

It depends on number of operations required to realize circuit. Actually complex constant complexity is assumed for each basic operation α for OR ,β for AND ,γ for NOT ,then total number of operations are calculated in terms of α, β, and γ
The reversible 5x32 decoder consists of a reversible 4x16 decoder and Fredkin gate which again consists of Peres gate, one TR gate, one NOT gate, three CNOT gates, 28 Fredkin gates

Table 1. Comparison between various Gates

Reversible gates	Quantum cost	Types
Feynman gate[23]	1	2*2
Toffoli gate[24]	5	3*3
Fredkin gate[6]	5	3*3
Peres gate[7]	4	3*3
TSG gate[25]	4	4*4
URG gate[26]	unknown	3*3
System gate[27]	unknown	4*4
TR gate[26]	6	3*3
NFT gate[26]	5	3*3
BJN gate[26]	5	3*3
MTSG gate[25]	6	4*4
BME gate[26]	5	4*4
Sayem gate[13]	unknown	4*4
VB-1 gate[28]	unknown	4*4
VB-2 gate[28]	unknown	4*4
MKG gate[29]	unknown	4*4

It is defined as the cost of the circuit in terms of cost of primitive gate .it is calculated by the number of primitive reversible gates (1x1 or 2x2) required to realize logic function. Quantum cost of circuit is the minimum number of 2x2 unitary gates required to keep output to be unchanged.

NOT gate: This is simplest gate with quantum cost zero

CNOT gate: It is known as controlled –not gate, it is a 2x2 reversible gate and is quantum cost is 1.

Feynman gate: It is controlled gate widely used for fan-out purposes.

Toffoli gate: It is a 3x3 gate its quantum cost is 5.

Fredkin gate: It is 3x3 Fredkin gate and its quantum cost is 5.

Peres gate: It is a 3x3 gate and its quantum cost is 4.

TR gate: It is a 3x3 reversible gate its quantum cost is 4

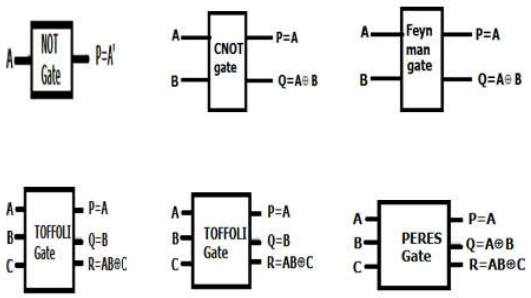

Fig.1: Reversible gates

PROPOSED REVERSIBLE 5X32 DECODER

For 32-bit and 64-bit processor there is a need to implement decoder capability, in this thesis decoder is implemented with reversible gates .Implementation is done using 4x8 decoder which is designed with 3x8 decoder integration smaller decoder stages to design higher decoders advantages the implementation with less gates. The reversible 5x32 decoder consists of a reversible 4x16 decoder and Fredkin gate which again consists of Peres gate, one TR gate, one NOT gate, three CNOT gates, 28 Fredkin gates.

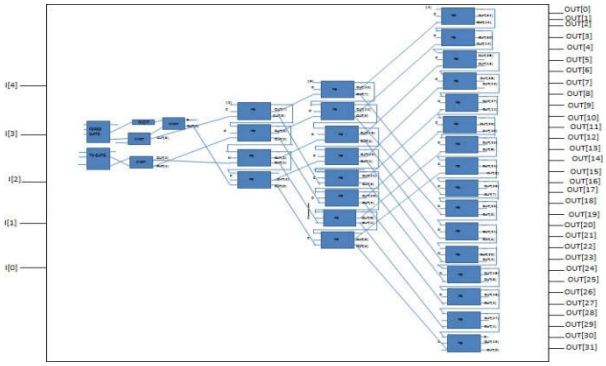

Fig.2. Diagram of 5*32 Decoder

Proposed 5x32 decoder operates on 5 inputs and gives 32 outputs, it is designed with reversible gates 28 Fredkin gates are given with 28 binary inputs and 5 inputs are given to decoder inputs total there are 33 inputs along with one garbage input for the reversible decoder .the outputs Fredkin gate given to other Fredkin gates, so from each Fredkin gates 2 outputs are obtained. Shown diagram is divided in to three segments, first segment consists four Fredkin gates with 8 outputs resembles the 3x8 decoder, in second segment there are eight Fredkin gates with four inputs from 3x8 decoder and so there are 16 outputs are available from eight Fredkin gates, this segment resembles 4x16 decoder with two garbage inputs and one garbage output, third segment consists of 16 Fredkin gates by taking 4x16 decoder outputs as inputs and generates 33 outputs considering one output as garbage output. Designed 5x32 decoder consists 32 input and 32 outputs for one to one mapping along with these three garbage inputs and three garbage outputs are present. The designed decoder highly preferred in quantum computation due to low power consumption and lower delay. Reversible computing may have applications in computer security and transaction processing but mainly in some areas they are proffered due to their energy efficiency and speed performance few applications are low power VLSI, Nano Technology, Optical computing, Computer graphics, FPGA Technology etc.

RESULTS

Reversible 5x32 decoder is designed using 4x16 Decoder Reversible decoder 5x32 is designed with 4x16 decoder and Fredkin gate using Xilinx ISE design suite with verilog.

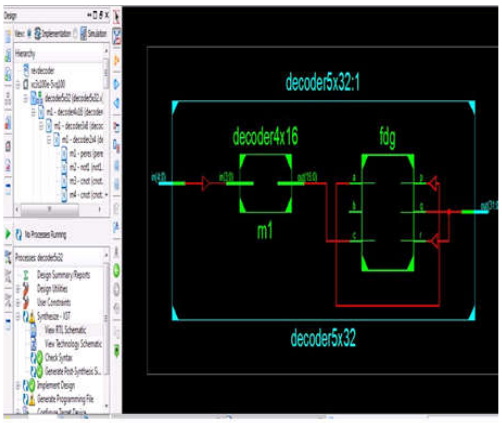

Fig.3: Diagram of 5*32 Decoder

Fig.4. Simulation results of 5*32 Decoder

CONCLUSION

Reversible gates in which the number of outputs equal to number of inputs and each must give equal output pattern. It also helps recovering inputs from outputs. Reversible decoder 5x32 is designed with 4x16 decoder and Fredkin gate with minimum cost, both delay and power consumption are reduced compared to normal decoder, with this 5x32 decoder many combinational and sequential circuits like full adder, multiplexer .., can be designed with less gates and quantum cost. Reversible decoder can be used in low power VLSI, DSP, Nano computing, optical computing.

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