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RESEARCH ARTICLE

DESIGN AND SIMULATION OF CASCADED SEVEN LEVEL INVERTER BASED ON STATCOM

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ABSTRACT

This paper is dedicated to the modelling and analysis of seven level inverter based on STATCOM. It presents a comprehensive study of static synchronous compensator (STATCOM) systems utilizing cascaded multilevel inverters. Among flexible AC transmission system (FACTS) controllers, the STATCOM have shown feasibility compared with other shunt controllers in terms of cost effectiveness in a wide range of problem-solving abilities from transmission to distribution levels. In this, we have considered the cascaded H-bridge multilevel inverter (CHBMLI), Diode-clamped multilevel inverter and Capacitor-clamped multilevel inverter. The Comparison in these inverters is based on the synthesized output voltage and current waveforms, % THD present in the output voltage and each inverter is controlled by pulse width modulation (PWM) technique. To minimize the power demand and scarcity we have to improve the power extracting methods. From solar cells, multilevel inverter is used to extract power and it synthesizes the desired ac output waveform from several dc sources. To control the reactive power instantaneously, this system is modelled using the ABC coordinates which calculates the instantaneous reactive power. And, this paper focuses on improving the efficiency of the multilevel inverter and quality of output voltage waveform before applying the voltage on the load.

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INTRODUCTION

The concept of multilevel inverters has been introduced since 1975. The term multilevel began with the three level inverters (Jose Rodriguez, 2002). However, the elementary concept of a multilevel inverter is achieved from high power to use a series of power semiconductor switches with several lower voltages dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries and renewable energy like wind, solar and fuel cell are used as the multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends upon the rating of the dc voltage sources only to which they are connected. Inverters are used to provide power to electronics in the case of a power outage or for activities such as camping, where no power is available. An inverter is used to convert a direct current (DC) or battery power into an alternating current (AC) or household power. Therefore, A multilevel inverter is play an important role for more powerful inverter, meaning it does the same thing as an inverter except provides energy in higher power situations (Suryanarayan, 2005).

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Therefore, inverter converts DC power into AC power through waves called either sine waves or modified sine waves. Sine waves are the waves that are typically found in power from a power plant and modified sine waves are made to simulate sine waves. Inverters with modified sine waves work well for backup power in houses and are much less expensive. Although there are different types of inverters, all standard inverters use only one switch or one power circuit. Unlike standard inverters, multilevel inverters make use of renewable energy sources. Wind, solar photovoltaic and fuel cells energy can be added to a multilevel inverter as DC sources. These environmentally-friendly energy sources can then be converted into AC currents. While multilevel inverters are capable however of producing large amounts of energy, the amount of energy produced is dependent upon how much DC power is being used. Higher sources of DC power will provide more powerful AC power. As compared with direct running power lines, amultilevel power converter system is a simpler solution for different voltages. There are three structures for multilevel inverters:

Cascaded H-Bridges (CHB)

In Figure 1, DC power source is connected to an H-bridge inverter. The single inverter has four switches. By using different combinations of switches, the single inverter can produce three different AC voltage outputs, +Vdc, 0, -Vdc.

Table 1. Switching Pattern for H-bridge Inverters

Sequence of Switches (ON)	Load Voltage
S_1, S_4	$+V_{dc}$
S_2, S_3	$-V_{dc}$
S_1, S_4 or S_2, S_3	Zero

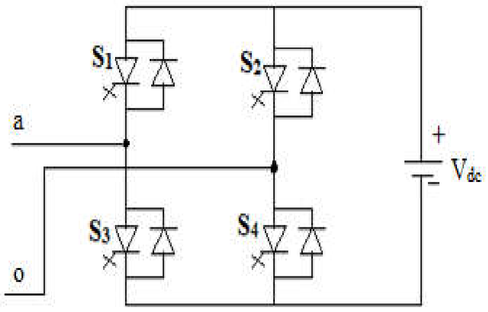


Figure 1. H-Bridge Inverter

Diode-Clamped Multilevel Inverter

This type of inverter is suitable on an AC transmission line for transmission of DC current or variable speed motors. Precise monitoring and control are required to prevent overcharging or discharging.

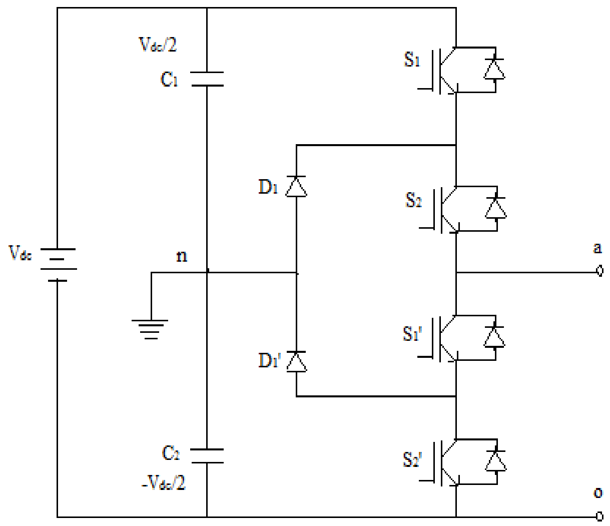


Figure 2. Three level Diode-clamped Inverter

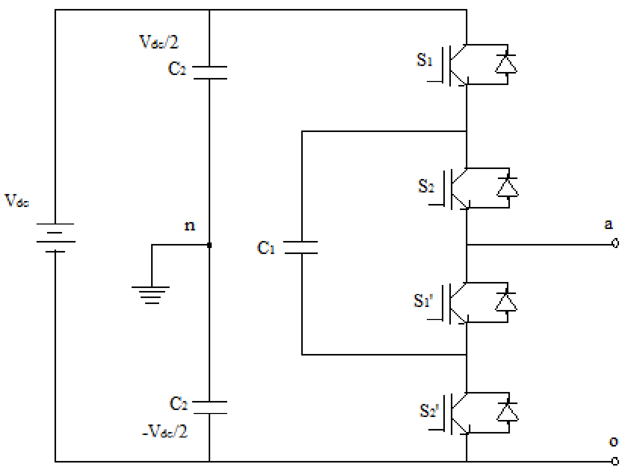


Figure 3. Three level Capacitor – clamped Inverter

Table 2. Switching pattern for 3-level Diode-Clamped inverters

Sequence of Switches (ON)	Load Voltage
S_1, S_2	$+V_{dc}/2$
S_1', S_2'	$-V_{dc}/2$
S_2, S_1' or S_1, S_2'	Zero

In Figure 2, the dc output voltage is split into three levels by two bulk capacitors C_1 and C_2 in series form. The middle point of the two capacitors 'n' is called the neutral point. These two diodes D_1 and D_1' clamp the switch voltage to half the level of the dc-bus voltage. When switches S_1 and S_2 turn on, the voltage across *a* and 0 is V_{dc}, i.e., $V_{ao}= V_{dc}$. In this case, D_1' balances out the voltage sharing between S_1' and S_2' with S_1' blocking the voltage across and blocking the voltage across C_1 and S_2' blocking the voltage across C_2. Notice that output voltage V_{an} is ac, and V_{ao} is dc. The difference between V_{an} and V_{ao} is the voltage across C_2, which is $V_{dc}/2$. If the output is removed out between *a* and 0, then the circuit becomes a dc/dc converter, which has three output voltage levels: V_{dc}, $V_{dc}/2$, and 0 as shown in Table 2.

Capacitor-Clamped Multilevel Inverter: This inverter has a similar design to a diode-clamped inverter. The clamping diodes have however been replaced with capacitors. The design requires only two switch combinations to create a voltage output. Tracking the output of all the capacitors is complicated, as is pre-charging all of the capacitors (Jose Rodriguez, 2002).The inverter in Figure 3 provides a three-level output across *a* and*n*, i.e., $V_{an}= V_{dc}/2$, 0, or $–V_{dc}/2$. For voltage level $V_{dc}/2$, switches S_1 and S_2 need to be turned on; for $–V_{dc}/2$, switches S_1' and S_2' need to be turned on; and for the 0 level, either pair (S_1,S_1') or (S_2,S_2') needs to be turned on. Clamping capacitor C_1 is charged when S_1 and S_1' are turned on, and is discharged when S_2 and S_2' are turned on. The charge of capacitor C_1 can be balanced by proper selection of the zero-level switch combination. Right now, for researchers and manufacturers, the multilevel inverter is become more attractive due to their advantages over conventional three-level pulse width modulation technique (PWM) inverters. Multilevel inverter topology has the minimum components for a given number of levels. Cascaded H-bridge MLI topology is based on the series connection of H-bridges with separate dc sources. Since the output terminals of the H bridges are connected in series, the dc sources must be isolated from each other. The need of several sources on the dc side of the inverter makes multilevel technology attractive for photovoltaic applications. Owing to this property, CHB-MLIs have also been proposed in order to achieve higher levels (Jose Rodriguez, 2002). For simplicity of the circuit and advantages, Cascaded H-bridge topology is chosen for the simulation work.

Objective

The objective is to come out with a simulation model of STATCOM based cascaded seven level inverter and analyzes its operation.

Operating Principle of MLI

The number of voltage levels in a CHB inverter can be found by using m=2s+1 where's' is the number of dc power sources. The voltage level 'm' is always an odd number for the CHB inverter. Therefore, the total number of CHB inverters can be calculated by n_{sw}=6(m-1) =6(7-1) = 6(6) = 36 for three phase

(Ahmad FaizMinai, 2011).Each 1-Φ H-bridge generates three voltage levels as $+V_{dc}$, 0, $-V_{dc}$ by connecting the dc source to the ac output by different combination of four switches for dc source V_1.

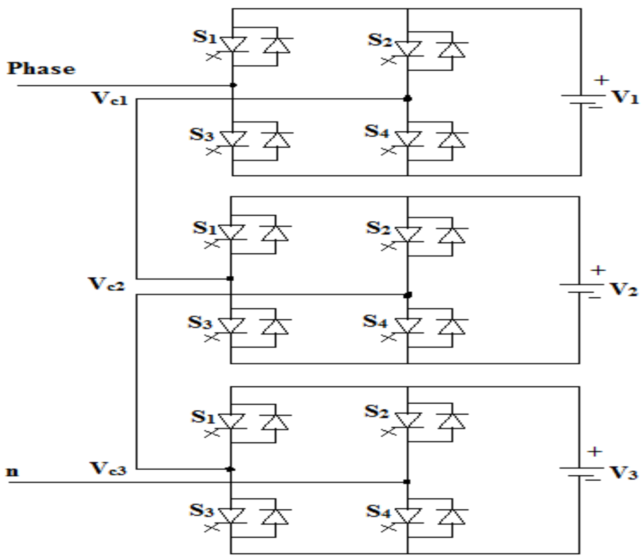


Figure 4. 1-Φ 7-level Cascaded Multilevel Inverter

The 3-Φ 7-level cascaded H-bridge inverter topology is realized using MATLAB/Simulink. The use of cascaded H-bridge multilevel inverter reduces the total harmonic distortion (THD) in the current waveform by increase in the number of levels of the output voltage and we can increase the number of levels of the inverter to reduce the harmonics.

AC component is achieved using Pulse Width Modulation (PWM) and the desired average value is controlled by modulating the width of the pulses (Suryanarayan, 2005). When we deal with three level or higher levels in inverter output, Multicarrier PWM is used. Multilevel PWM is basically a generalization of the 2-level PWM wherein the sinusoidal reference signal is naturally sampled with the help of a number of carrier signals.

Cascaded Multilevel Inverter with STATCOM

A 7-level, 3-Φcascaded multilevel inverter based on STATCOM configuration is illustrated in Figure 6. It illustrates the connection diagram for a wye connection seven level inverter using the cascade voltage source H-bridge inverter. Figure 7 shows the structure of one unit of H-bridge inverter. Each HBI can generate three level output, $+V_{dc}$, o and $-V_{dc}$. In figure 8, when the inverter output voltage (V_c) is higher than the ac system voltage (V_s), leading reactive current is drawn from the system (vars are generated). When the inverter output voltage (V_c) is lower than the ac system voltage (V_s), the lagging reactive current is drawn from the system (vars are absorbed). When the inverter output voltage is equal to the AC system voltage reactive power exchange is zero and it shows a 1-Φ equivalent circuit of the STATCOM, where V_s is the source voltage phasor, V_c is ac output of STATCOM, and L and R represent respectively a set of linked AC reactor and equivalent resistance including STATCOM losses. The voltage controlled STATCOM for AC system can control the amplitude of AC voltage by causing a small amount of active power to power flow into or out of the STATCOM. Figure 9 shows a phasor diagram in the case that V_c lags Vs, it is in

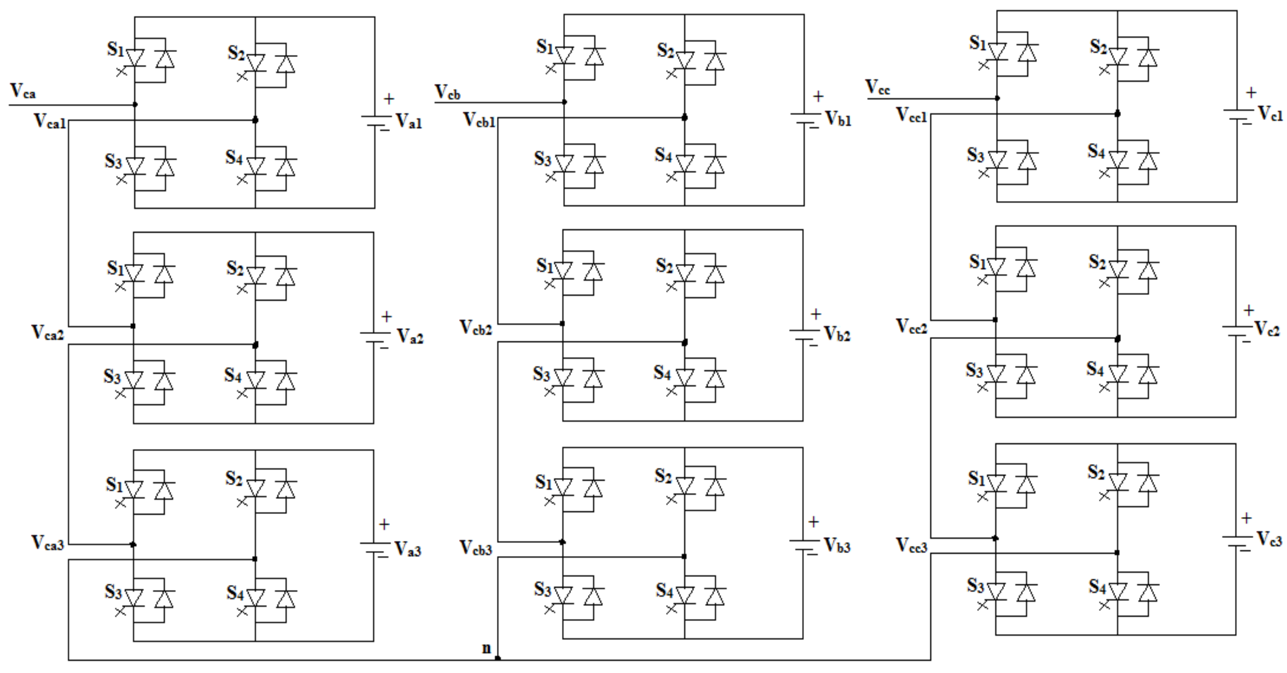


Figure 5. 3-Φ 7-level Cascaded Multilevel Inverter

Control Technique

Importantly, the power electronic converters are operated in the "switched mode". The switches of the converter are always in either one of the two states - OFF (no current flows), or ON (saturated with only a small voltage drop across the switch) (Tolbert,, 1999 and Meynard and Foch, 1992). The switched component is attenuated and the desired DC or low frequency

phase with V_s and in the case where V_c leads V_s, a small amount of active power flows in both cases. Therefore, a reactive power in large amount is drawn by the STATCOM and can be controlled by adjusting the phase angle by the small amount.

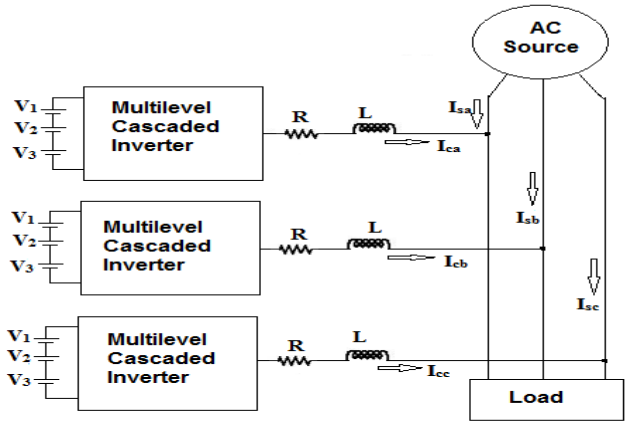


Figure 6. Structure of the STATCOM with Cascade Multilevel Inverter

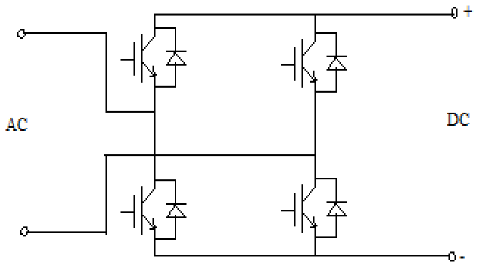


Figure 7. H-Bridge inverter with IGBT/diode

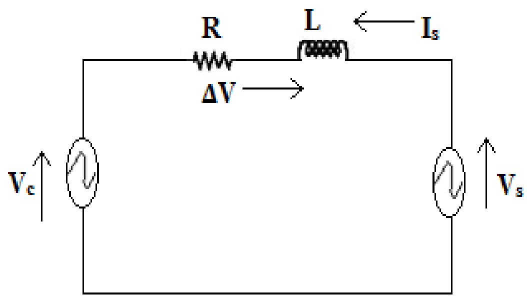
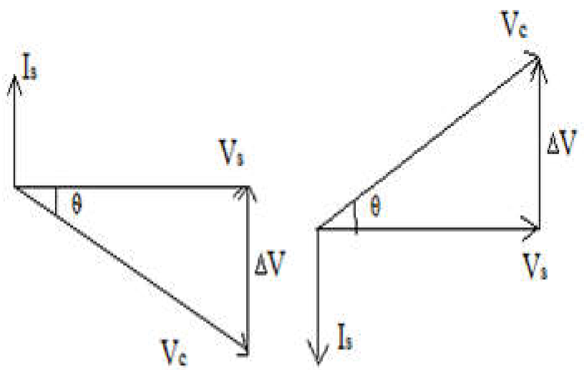


Figure 8. Single phase equivalent circuit



(a) Leading current (b) Lagging current

Figure 9. Phasor diagram of the STATCOM

SYSTEM MODELING

From Figure 5.1, the ideal three phase power supply is given by-

$$\begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} = \sqrt{\frac{2}{3}} V_{sl} \begin{bmatrix} \sin(\omega t) \\ \sin(\omega t - 2\pi/3) \\ \sin(\omega t + 2\pi/3) \end{bmatrix} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(1)$$

Where the V_{sl} and ω denote the rms line to line voltage and frequency of source voltage. Using the Figure 6, one obtains the following equation.

$$\begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} = \left(R + L\frac{d}{dt}\right) \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} + \begin{bmatrix} V_{ca} \\ V_{cb} \\ V_{cc} \end{bmatrix} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(2)$$

Under the assumption that harmonic components generated by switching pattern are negligible, the switching function S can be defined as follows:

$$S = \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} = \sqrt{\frac{2}{3}} M \begin{bmatrix} \cos(wt+\propto) & \cos\left(wt+\propto - \frac{2}{3}\pi\right) & \cos\left(wt+\propto + \frac{2}{3}\pi\right) \\ \sin(wt+\propto) & \sin\left(wt+\propto - \frac{2}{3}\pi\right) & \sin\left(wt+\propto + \frac{2}{3}\pi\right) \\ \sqrt{\frac{1}{2}} & \sqrt{\frac{1}{2}} & \sqrt{\frac{1}{2}} \end{bmatrix} \ldots\ldots\ldots(3)$$

Where ∝ is the phase angle which relates the phase difference between output voltage of source voltage and cascade multilevel inverter.

The modulation index is given by:

$$M = \frac{V_{c,peak}}{3V_{dc}} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(4)$$

Now, the output voltage of the cascade multilevel inverter and capacitor DC current can be expressed as follows:

$$V_{c,abc} = S \times 3V_{dc} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(5)$$

$$i_{dc} = S^T i_{abc} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(6)$$

Control of reactive power

It is well satisfied that the amount and type (capacitive or inductive) of reactive power exchange between the STATCOM and the system can be adjusted by controlling the magnitude value of the output voltage for STATCOM with respect to that of system supply voltage. The reactive power supplied by the STATCOM is given by equation (7),

$$Q = V_{statcom} - V_s \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(7)$$

Where, $V_{statcom}$ and V_s are the magnitudes of STATCOM output voltage and system voltage respectively and X is the equivalent reactance between STATCOM and the system. The STATCOM supplies reactive power to the system, when reactive power is positive,. Otherwise, STATCOM absorbs reactive power from the system.

SIMULATION AND RESULTS

Figure 12 shows the load current and output voltage waveform of a single phase H-bridge inverter when the load is RL. For RL load, load current will not be in phase with output voltage and diodes connected in antiparallel with IGBTs will allow the current to flow when the main IGBTs are turned off.

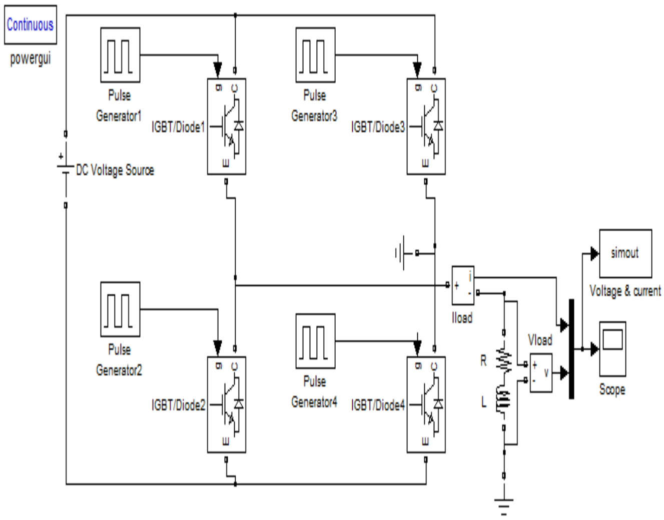


Figure 10. Simulated 1-Φ Bridge inverter

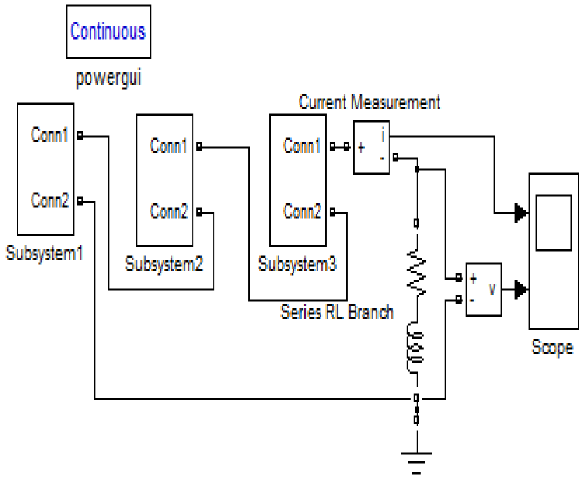


Figure 11. Simulated Circuit for 1-Φ Cascaded 7-level Inverter

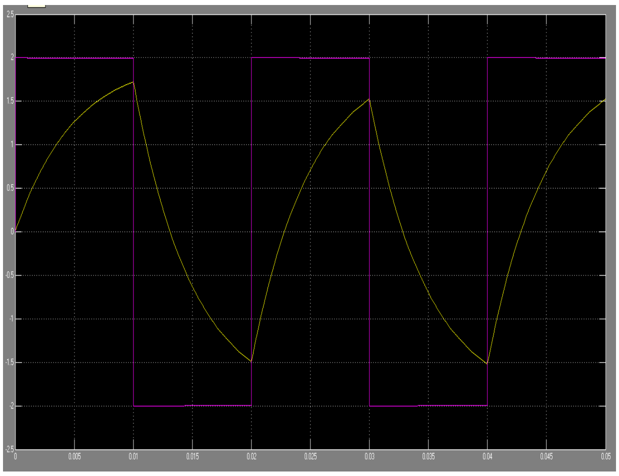


Figure 12. Load current v/s time

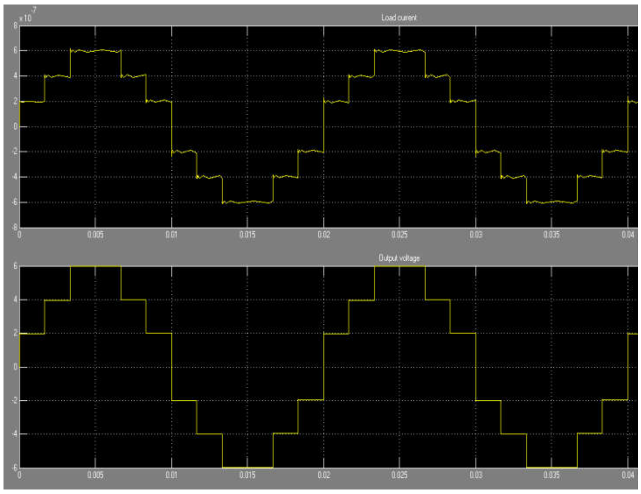


Figure 13. Simulated 1-Φ Cascaded 7-level Inverter Output Current and Voltage Waveform

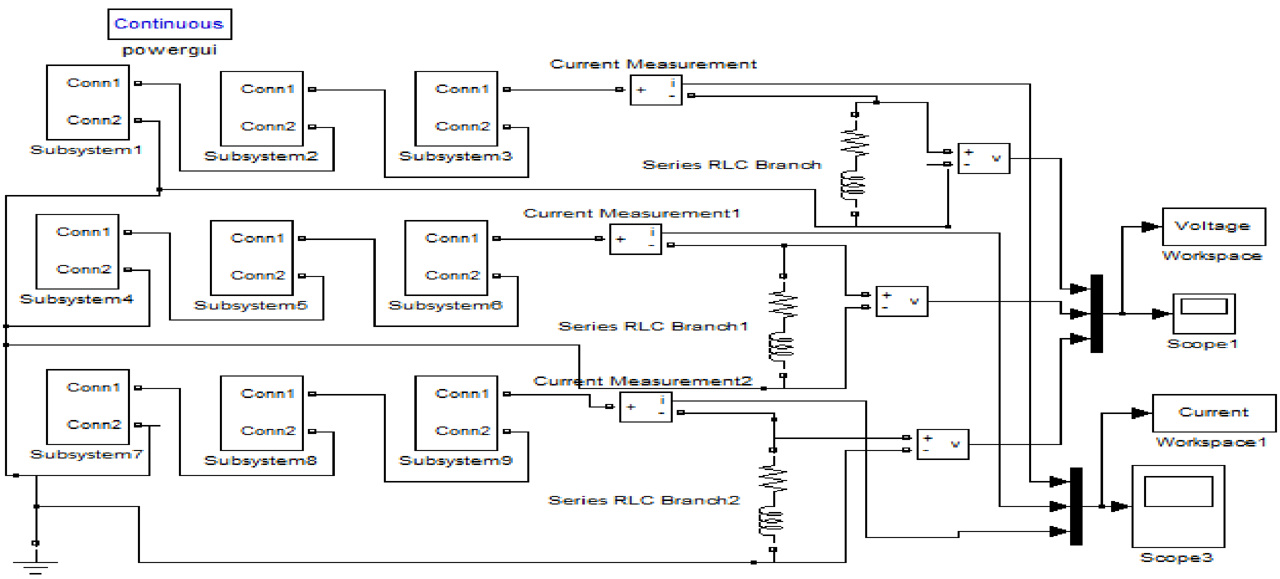


Figure 14. Simulated Circuit for 3-Φ Cascaded 7-level Inverter

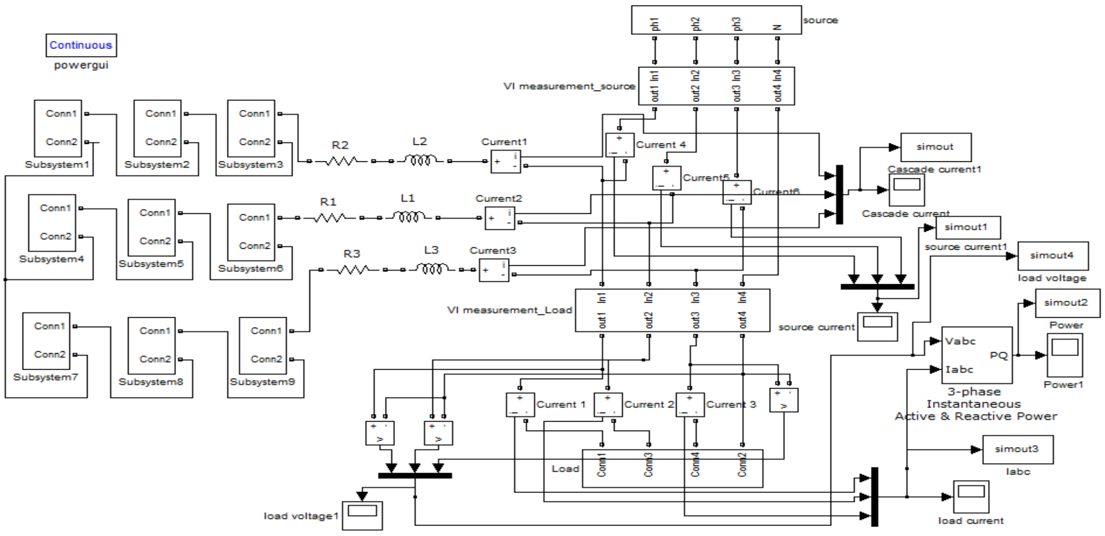


Figure 15. Simulated Circuit for 3-Φ Cascaded Seven level Inverter with STATCOM

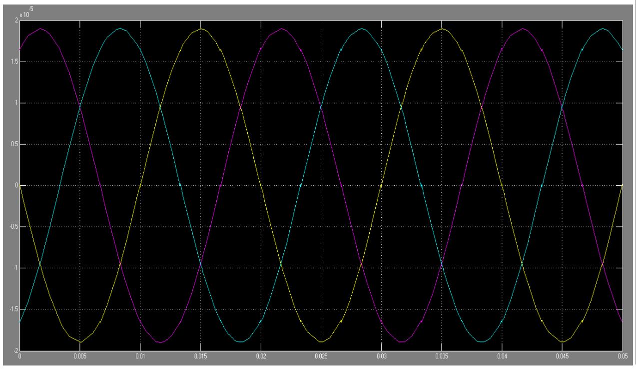


Figure 16. 3-Φ Cascade output current in STATCOM v/s time

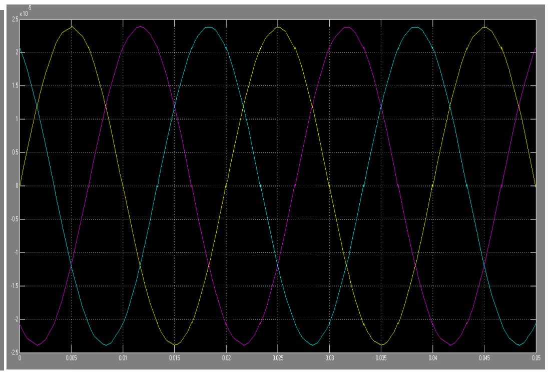


Figure 17. 3-Φ ac supply current in STATCOM v/s time

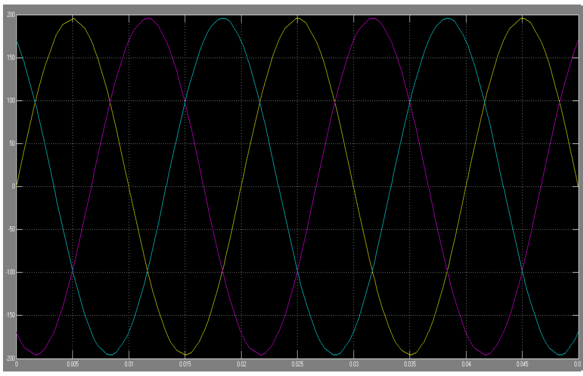


Figure 18. 3-Φ Load Voltage in STATCOM v/s time

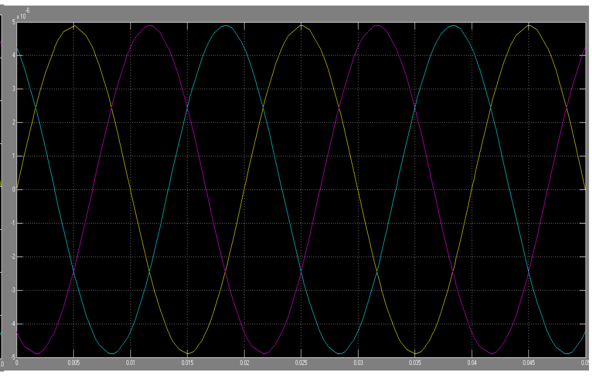


Figure 19. 3-Φ Load Current in STATCOM v/s time

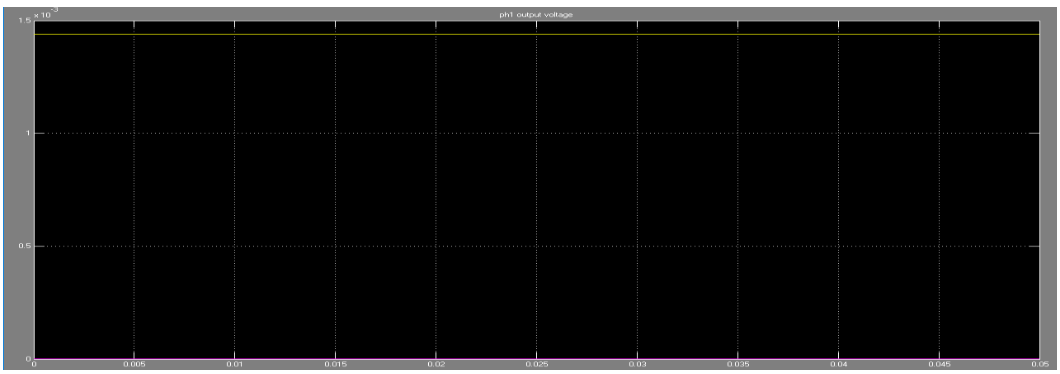


Figure 20. Active and Reactive power in 3-Φ Cascaded 7-level Inverter based STATCOM

Conclusion

In conclusion, among the nature multilevel inverter topologies, the cascaded multilevel inverter is the most promising alternative for the STATCOM application and it requires the least number of switches as compared to other topologies to achieve the same number of output voltage levels. However, the control complexity of the cascaded multilevel inverter is directly proportional to the number of H-bridge inverters. In the STATCOM applications, the DC supply voltage is used to find its AC voltage of each H-bridge inverter which needs to be individually regulated. The voltage-imbalance problem becomes more of a concern for the number of voltage levels increases. The source voltage, cascade voltage, load voltage, source current, cascade current and load current simulation results are presented. Finally, Matlab/Simulink based model for cascaded Seven level inverter based on STATCOM is developed and simulation results are presented.

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